BRANCH :ELE SEMESTER :5TH NO OF CLASSES/W: 3 GROUP :1/2	LESSON PLAN SUB: DE &MP LAB FACULTY NAME: NIHARIKA SETHY , ECT- ETC SEMESTER START: FROM 14.07.2025 TO 15.11.2025 Total No of weeks:18	
WEEK	TOPICS TO BE COVERED	STATUS
W1	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.	
W2	Implement various gates by using universal properties of NAND & NOR gates andverify truth table.	
W3	Implement half adder and Full adder using logic gates	
W4	Implement half subtractor and Full subtractor using logic gates.	
W5	Implement a 4-bit Binary to Gray code converter	
W6	Implement a Single bit digital comparator	
W7	Study Multiplexer and de multiplexer.	
W8	Study of flip-flops. i)S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop	
W9	Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting.	
W10	Realize a 4-bit synchronous UP/Down counter with a control for up/down counting.	
W11	Implement Mode-10 asynchronous counters.	
W12	Study shift registers	
W13	a. 1'S Complement. b. 2'S Complement. a. Addition of 8-bit number. b. Subtraction of 8-bit number resulting 8/16 bit number.	
W14	a. Decimal Addition 8-bit number. b. Decimal Subtraction 8-bit number	
W15	a. Find the largest in an Array	
W16	b. Compare between two numbers , Block Transfer.	
W17	Traffic light control using 8255.	
W18	Generation of square wave using 8255