Thyristor

Thyristor is a hard semiconductor switching device and it's function is to control the power in A.C. and D.C. circuits. Thyristors are family of power semiconductor device. They are operated as bistable switches, operating from non-conducting state to conducting state.

→ It is first introduced by Bell laboratory (USA) in 1957. It is a unidirectional device.

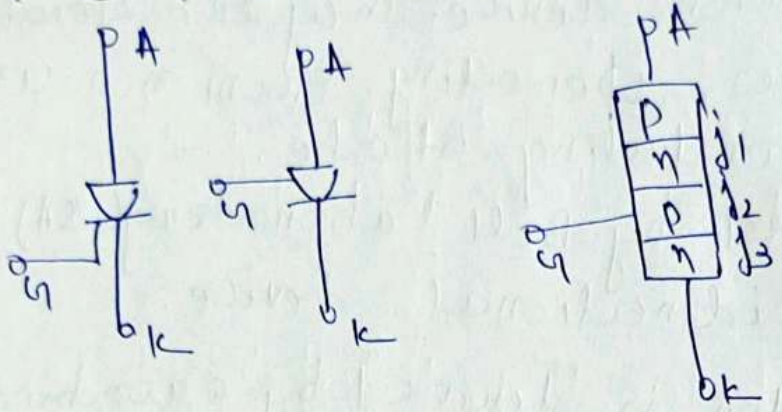
→ The name thyristor is derived by a combination of letters from THYRatron and transISTOR. This means thyristor is a solid state device like a transistor and has characteristics similar to that of thyratron tube.

→ Conventional thyristors (CTs) are designed without gate-controlled turn-off capability. Thyristors can recover from its conducting state to a nonconducting state only when the current is brought to zero by some means or anode current lower below holding current. Gate turn-off thyristors (GTOs) are designed to have both controlled turn-on and turn-off capability.

→ Compared to transistors, thyristor have lower on-state conduction losses and higher power handling capability. Transistors generally have superior switching performance in term of faster switching speed & lower switching losses.

→ SCR is one oldest member of thyristor family. It is the most widely used device.

→ An SCR is so called bcz silicon is used from it's construction and it's operation as a rectifier it can be controlled.



A SCR is a 4-layer, 3-junction P-n-P-n semiconductor switching device. It has three terminals anode, cathode and gate. SCRs of voltage rating 10kV and rms current rating of 3kA with power-handling capacity of 30MW are available.

Static V-I Characteristics of thyristor.

Thyristor have three mode of operation:-

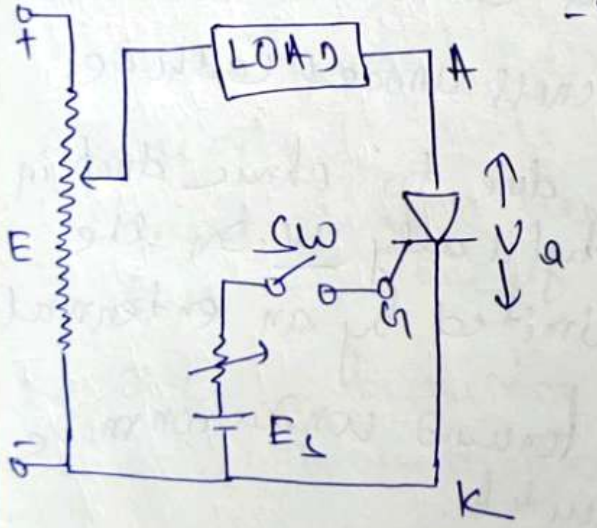
1. Reverse blocking mode
2. Forward blocking mode
3. Forward conduction mode.

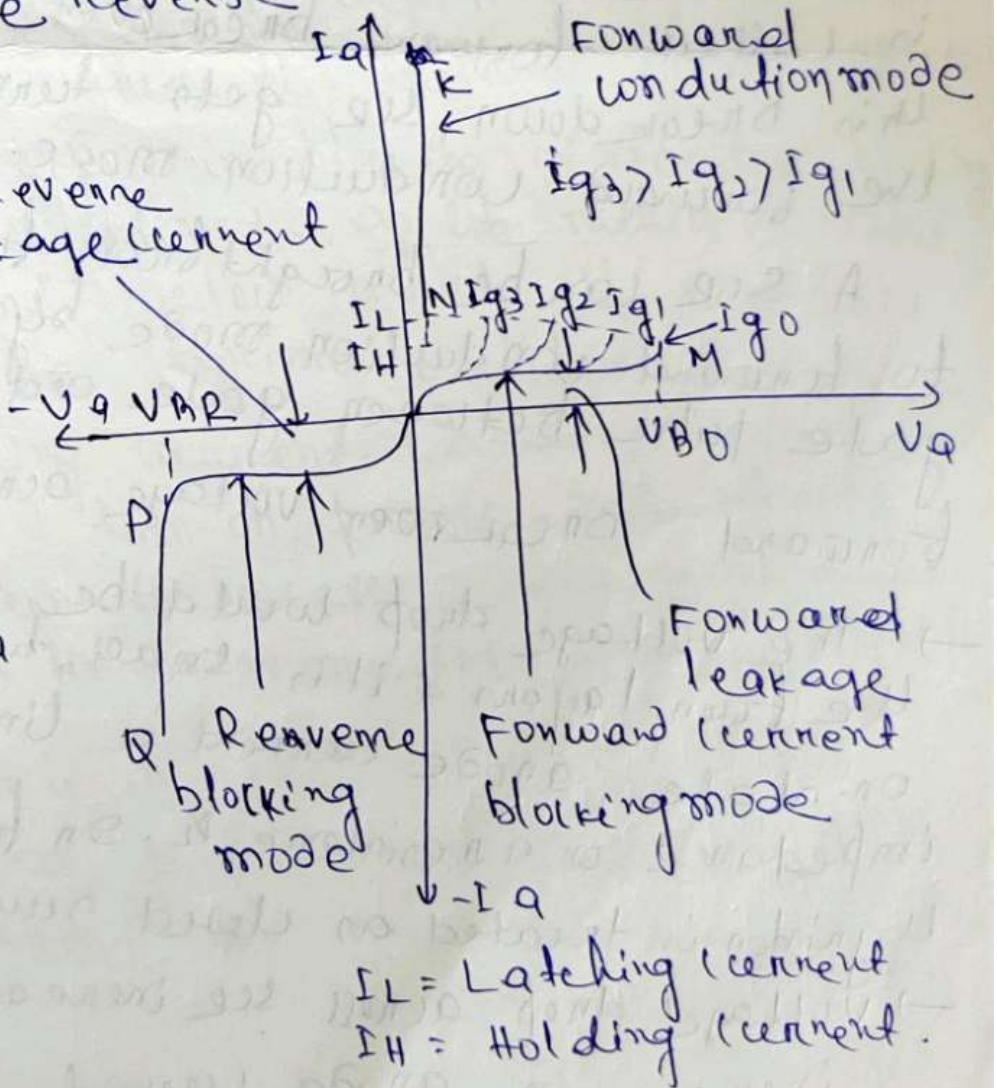
Reverse blocking mode.

When cathode is made +ve w.r.t. anode, the junction J_2 is forward biased but junction J_1 & J_3 are reverse biased. The device behaves as if two diodes are connected in series with reverse voltage across them.

A small leakage current of few milliamperes flows in the device. This is reverse blocking mode, called the off-state. Reverse blocking mode is shown by OP.

→ If the reverse voltage is increased, then at a critical breakdown level, called reverse breakdown voltage V_{BR}, an avalanche occurs at J1 & J3 and reverse current increases rapidly. This may cause thyristor damage as the junction temperature may exceed its permissible temperature rise. It should therefore ensure that maximum working reverse voltage across the device does not exceed V_{BR}. The SCR in the reverse blocking mode may be treated as open switch because the device offers high impedance in the reverse direction.





I_L = Latching current
I_H = Holding current.

Forward blocking mode. When anode is +ve w.r.t cathode, with gate circuit open, SCR is said to forward biased. junction J_1 & J_3 are forward biased but junction J_2 is reverse biased. Only a small leakage current flows from anode to cathode. On reference forward blocking mode. Thyristor can be treated as an open switch even in forward blocking mode since SCR offers high impedance.

Forward conduction mode. When Anode is +ve w.r.t. cathode, if the anode to cathode voltage V_{AK} is increased to a sufficiently large value, the reverse bias junction J_2 breaks. This is known as avalanche breakdown and the corresponding voltage is called forward breakover voltage V_{BO}. After this breakdown, SCR gets turned on. NK. reference the forward conduction mode.

A SCR can be brought from forward blocking mode to forward conduction mode by applying (i) a +ve gate pulse between gate and cathode (ii) a forward breakover voltage across anode & cathode.

→ The voltage drop would be due to ohmic drop in the four layers & it is small, typically 1V. On the on-state, anode current is limited by an external impedance or a resistance R_L. On forward conduction mode thyristor is treated as closed switch.

→ Voltage drop across SCR increases slightly with an increase in anode current.

Anode current must be more than a value known as latching current to maintain SCR remain in on-state.

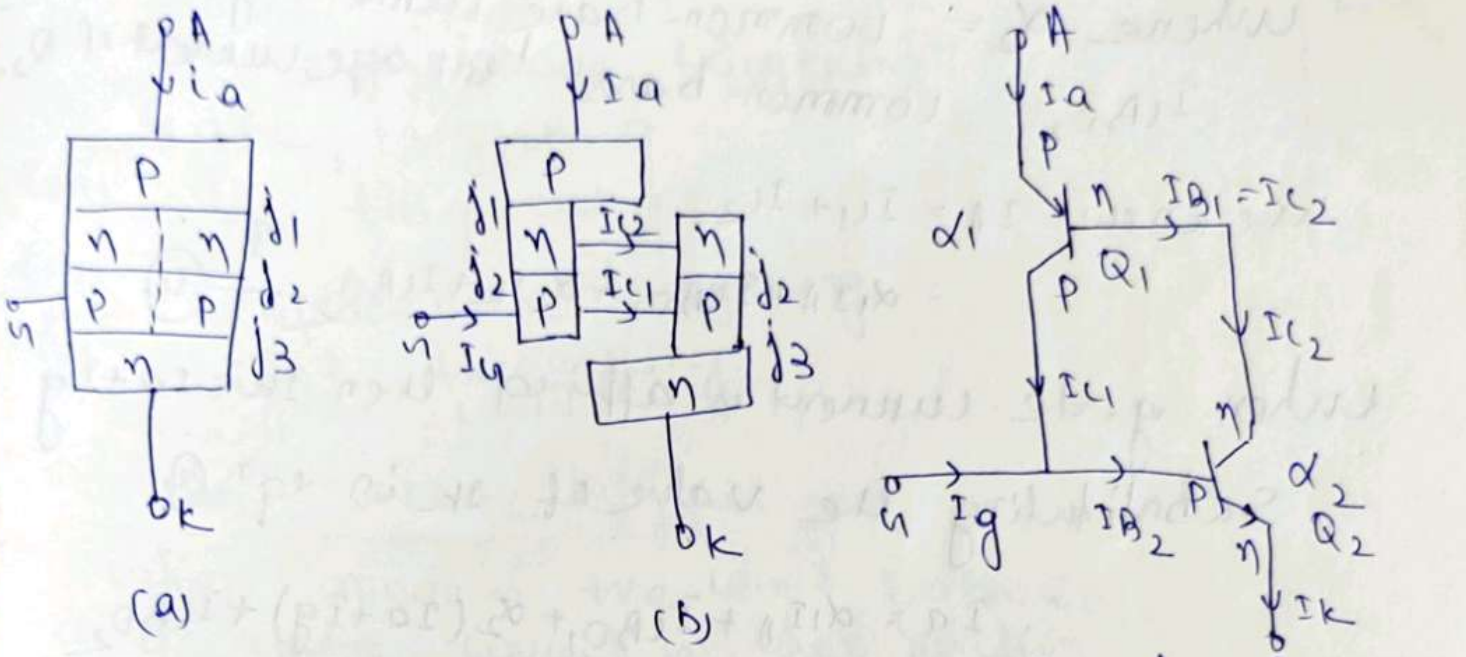
Latching current I_L is the minimum anode current required to maintain the thyristor in the on-state immediately after a SCR has been turned on & the gate signal has been removed.

→ once a thyristor conducts, it behaves like a conducting diode & there is no control over the device. The device continues to conduct bcz there is no depletion layer on the junction j_2 due to free movements of carriers. If the forward anode current is reduced below a level known as the holding current (I_H), a depletion region develops around junction j_2 due to reduced number of carriers & the SCR is in blocking state. Thus holding current may be defined as the minimum value of anode current below which it must fall for turning-off the thyristor. Latching current is higher than holding current. Latching current is associated with turn-on process and holding current with turn-off process. Latching current is two to three times more than holding current.

→ once thyristor is in conducting state, its gate signal is removed, it would remain in on-state ie. gate has no-control once SCR is conducting.

Two transistor model of thyristor

A thyristor can be considered as two complementary transistors, one pnp transistor Q_1 and other npn transistor Q_2 as shown below.



The collector current I_C of a ~~thyristor~~ transistor is related to emitter current I_E & the leakage current of the collector-base junction I_{CBO}, as

$$I_C = \alpha I_E + I_{CBO} \quad \text{— (1)}$$

where α is the common-base current gain & I_{CBO} is the common-base leakage current of collector-base junction of a transistor.

α is defined as $\alpha = \frac{I_C}{I_E}$

For transistor Q_1, $I_E = I_A$, then I_{C1} (collector current)

$$I_{C1} = \alpha_1 I_A + I_{CBO_1} \quad \text{— (2)}$$

where α_1 = common-base current gain of Q_1

& I_{CBO1} = common-base leakage current of

Similarly for transistor Q_2, collector current given by $I_{C2} = \alpha_2 I_K + I_{CBO2}$ — (3)

where α_2 = common-base current gain of Q_2

I_{CBO2} = common-base leakage current of Q_2.

we know $I_A = I_{C1} + I_{C2}$

$= \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2}$ — (4)

when gate current is applied, then $I_K = I_a + I_g$

Substituting the value of I_K in eqn (4),

$\therefore I_a = \alpha_1 I_A + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$

$\therefore \Rightarrow \boxed{I_a = \dfrac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2}}$ — (5)

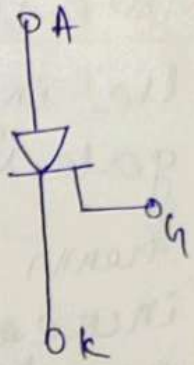
Neglecting leakage current I_{CBO1}, I_{CBO2}

we get $\boxed{I_a = \dfrac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2}}$ — (6)

when sum of α_1 and α_2 is unity, then the current 'Ia' tends to infinite which turns on the device.

Thyristor Turn-on Methods

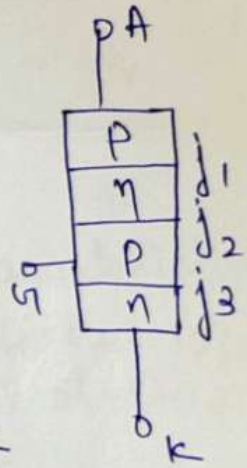
When anode is positive w.r.t. cathode, a thyristor can be turned on by any one of the following methods.



(i) Forward voltage triggering
(ii) Gate triggering
(iii) $\frac{dv}{dt}$ triggering
(iv) Temperature triggering
(v) Light triggering.

Forward voltage triggering

When anode is +ve w.r.t. cathode, and gate circuit is open, junction j_1 and j_3 are forward biased and j_2 is reverse biased. When anode to cathode forward voltage is increased junction j_2 will break. This is known as avalanche breakdown and the voltage at which avalanche occurs is called forward breakover voltage (V_{BO}). At this voltage, thyristor changes from OFF-state to ON-state. In practice the transition from off-state to on-state obtained by exceeding V_{BO} is never employed as it may destroy the device.



The magnitude of forward breakover and reverse breakdown voltage are nearly the same and both are temperature dependent. In practice, it is

found that V_{BR} is slightly more than V_{BO}.

Gate triggering of the thyristor is forward biased the injection of gate current by applying positive gate voltage between gate and cathode terminals turns on the thyristor. As the gate current is increased, the forward blocking voltage is decreased as shown below.

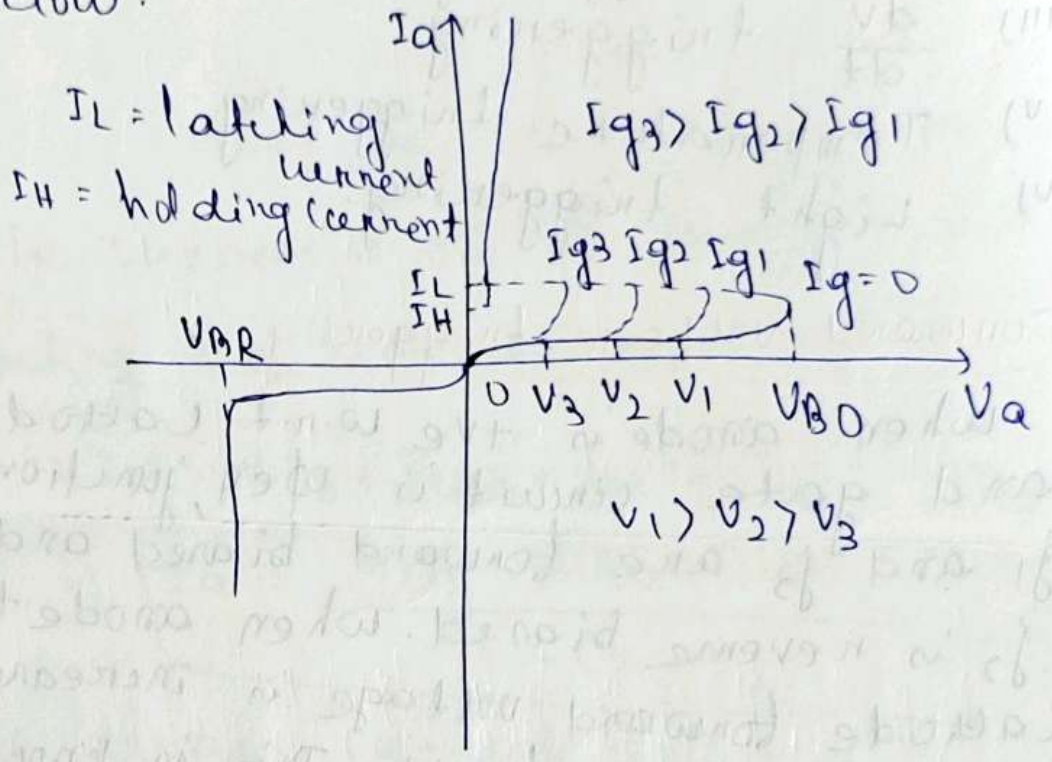


Fig- Effect of gate current on V_{BO}

The following points are considered in designing the gate control circuit.

(1) The gate signal should be removed after the thyristor is turned on. A continuous gating signal would increase the power loss in the gate junction.

(2) When the SCR is reverse biased, there should be no gate signal, otherwise, the thyristor may fail due to an increased leakage current.

The width of gate pulse t_g must be longer than the time required for the anode current to rise to holding current. In practice, the pulse width t_g is normally made more than the turn on time t_{on} of the thyristor.

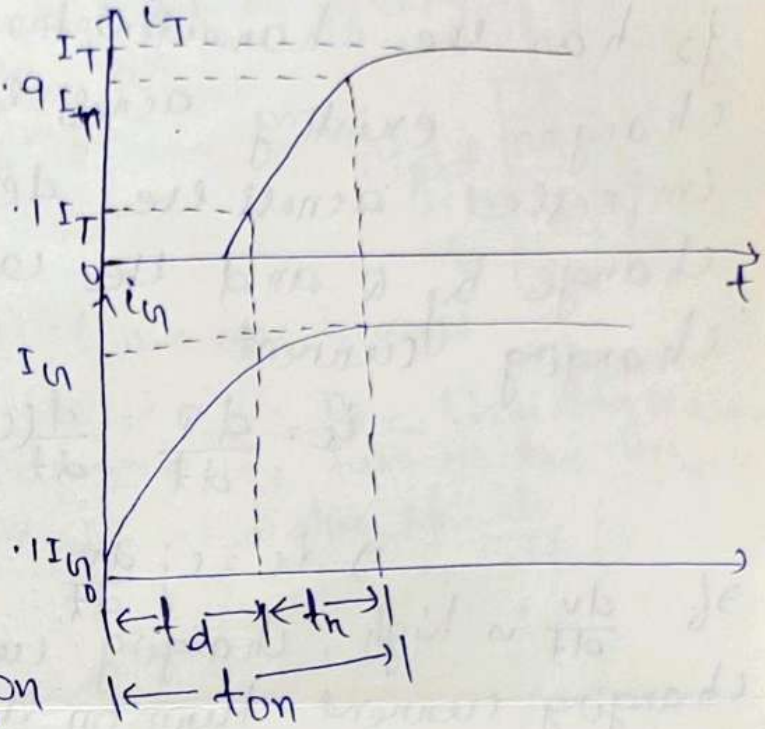


Fig. shows the waveform of the anode current, following the application of gate signal.

There is a time delay known as turn-on time t_{on} between the application of gate signal and the conduction of thyristor.

Fig - Turn on characteristics.

t_{on} is defined as the time interval between 10% of steady-state gate current ($.1I_G$) and 90% of the steady-state thyristor on-state current ($.9I_T$). t_{on} is the summation of delay time t_d & rise time t_r.

t_d is defined as the time interval between 10% of gate current ($.1I_G$) and 10% of thyristor on-state current ($.1I_T$).

t_r is the time required for the anode current to rise from 10% of on-state current ($.1I_T$) to 90% of on-state current ($.9I_T$).

Among all triggering, gate triggering is simple, reliable & efficient.

$\frac{dv}{dt}$ triggering

We know that with forward voltage across the anode and cathode of device, junction j_1 & j_3 are forward biased where as junction j_2 becomes reverse biased. This reverse biased junction j_2 has the characteristics of a capacitor due to charges existing across the junction. If the voltage impressed across the device is denoted by 'v', the change by Q and the capacitance by C_j, then the charging current

$$i_c = \frac{dQ}{dt} = \frac{d(C_j \cdot v)}{dt} = C_j \frac{dv}{dt} + v\frac{dC_j}{dt}$$

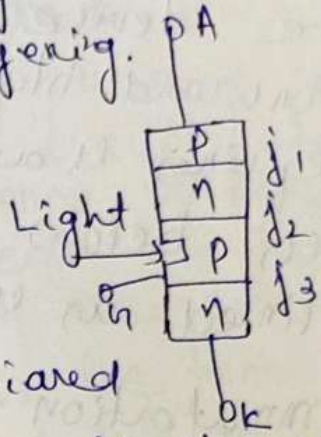
$$\Rightarrow i_c = C_j \frac{dv}{dt} \quad \text{as } C_j \text{ is constant.}$$

If $\frac{dv}{dt}$ is high, charging current i_c will be more. This charging current turn on the thyristor even when the gate signal is zero.

Temperature Triggering

During forward blocking mode most of the applied voltage appear across reverse biased junction j_2. This voltage across the junction associated with leakage current may raise the temperature of this junction which generate heat. which increases leakage current. This increase in currents ~~the~~ cause α_1 & α_2 to increase. Due to regenerative action, $(\alpha_1 + \alpha_2)$ may tend to unity & the thyristor may turn-on. This type of turn on may cause thermal run-away & is normally avoided. Here α_1 & α_2 are the common-base current gain of transistor one and transistor two respectively.

Light triggering. Light of appropriate wave-length is incident on the hole as shown in the figure, the electron-hole pairs increase and subsequently reverse junction j_2 break. So the thyristor is turned-on. This called light triggering. Such a thyristor is known as light-activated SCR (LASCR).



Problem. The capacitance of reverse-biased junction j_2 in a SCR is $C_{j2} = 20\,PF$. The limiting value of the ~~rate~~ changing current to turn on the thyristor is 16mA. Determine the critical value of $\frac{dv}{dt}$.

Soln.

given $C_{j2} = 20\,PF$

$i_c = 16mA$

We know $i_c = C_j \frac{dv}{dt}$

i.e. $\frac{dv}{dt} = \frac{i_c}{C_{j2}} = \frac{16 \times 10^{-3}}{20 \times 10^{-12}} = 800\,V/\mu s.$

Ans.

Thyristor turn-off For the purpose of power control & power conditioning, a conducting thyristor must be turned-off. The turn off a thyristor means bringing the device from forward conduction state to forward blocking state. The thyristor turn-off requires that at its anode current (forward current) falls below the holding current. Commutation is defined as the process of turning-off a thyristor.

Commutation may be of two types

① Natural or line commutation

② Forced commutation

Natural commutation. It is a turn-off process the SCR gets into the off state whenever the supply voltage passes through natural zero. This may be obtained whenever an ac input is given. Additional commutation circuit is not required for this natural commutation. This type of commutation process is used in A.C. voltage regulators, step-down cycloconverters.

Forced commutation. It is a turn-off process where the SCR gets into turn off state whenever the current flowing through the SCR is made zero for sometime by using external circuit. The commutating elements generally employed are inductor and capacitor. This type of commutation process is used for D.C. input circuits.

due to two outer Pn-junctions j_1 & j_3, the turn-off characteristics may be similar to that of a diode, exhibiting reverse recovery time t_{rr} and Peak reverse recovery current I_{RR}. I_{RR} can be much greater than the normal blocking current I_R. In a line-commutated converter circuit where input voltage is A.C., a reverse voltage appear across the thyristor immediately after the forward current goes through zero value. This reverse voltage accelerates the turn-off process, by sweeping out the excess carriers from Pn-junction T_1 & T_3.

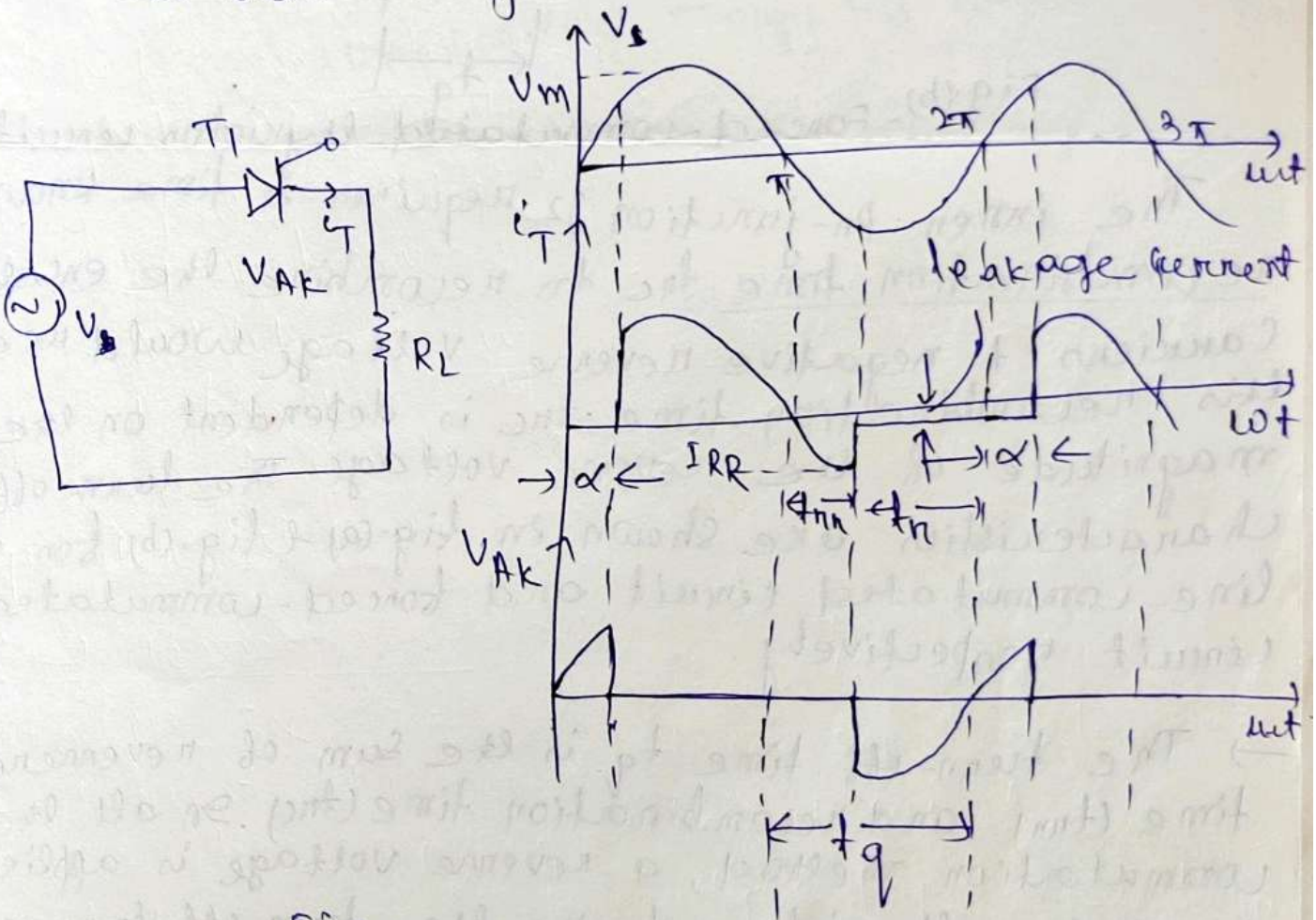


Fig.(a) Line-commutated thyristor ckt.

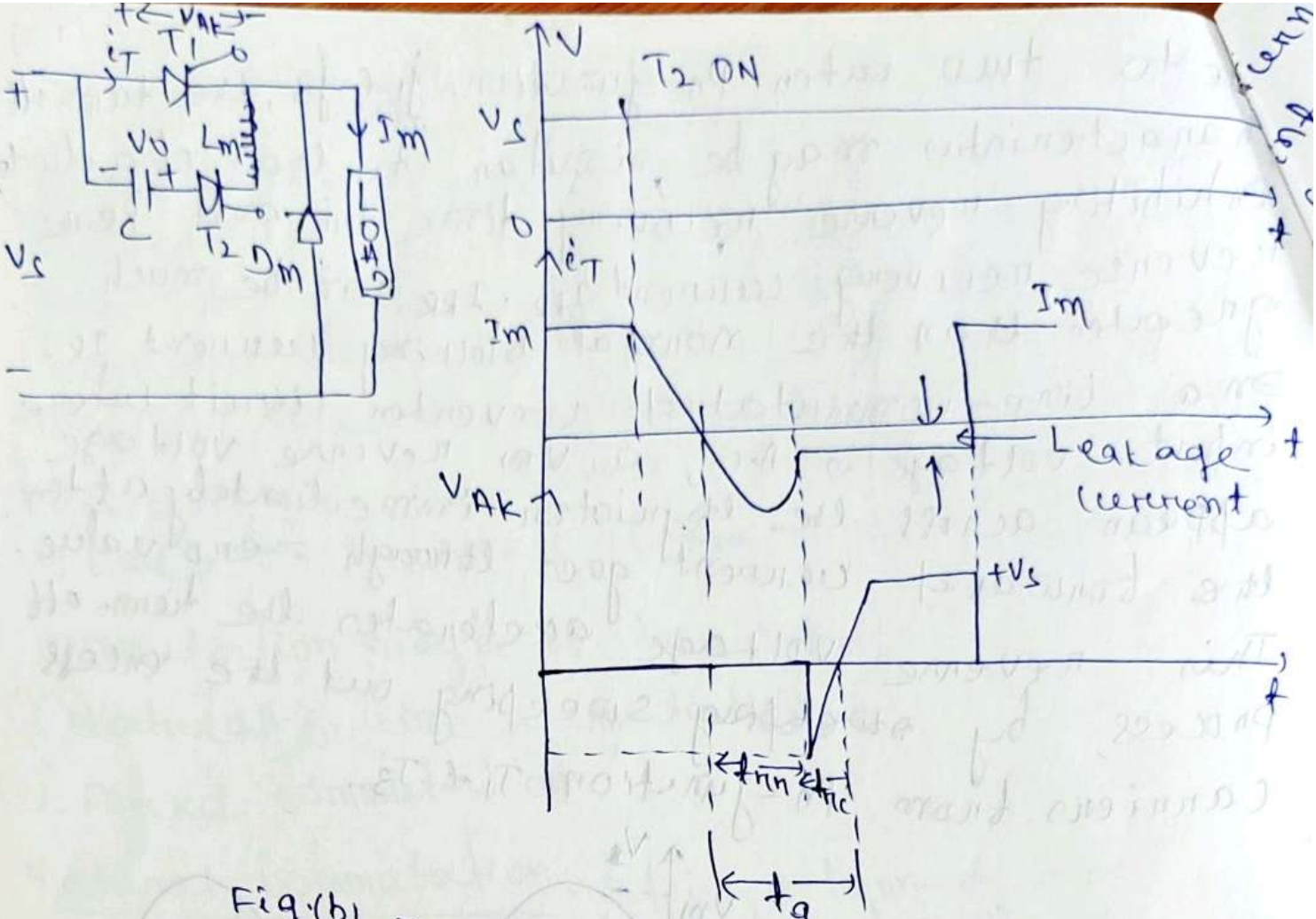


Fig.(b) - Forced-commutated thyristor circuit.

The inner Pn-junction j_2 requires a time known recombination time t_{rc} to recombine the excess carriers. A negative reverse voltage would reduce this recombination time. t_{rc} is dependent on the magnitude of the reverse voltage. The turn-off characteristics are shown in fig.(a) & fig.(b) for a line-commutated circuit and forced-commutated circuit respectively.

→ The turn-off time t_q is the sum of reverse recovery time (t_{rr}) and recombination time (t_{rc}). In all the commutation method, a reverse voltage is applied across the thyristor during the turn-off process.

Turn-off time t_q is the minimum value of time interval between the instant when the on-state current has decreased to zero and the instant when the thyristor is capable of withstanding forward voltage without turning on.
t_q depends on the peak value of on-state current and the instantaneous on-state voltage.

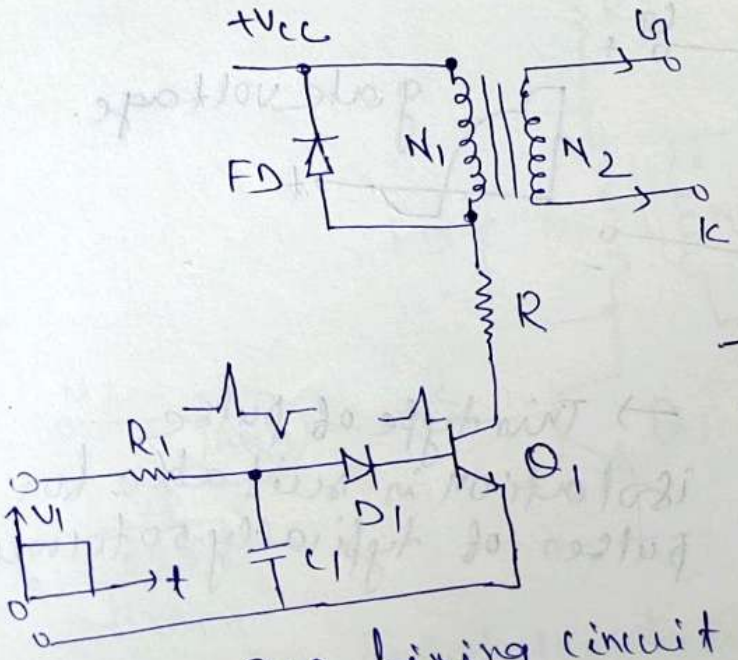
→ Reverse recovered charge Q_{RR} is the amount of charge that has to be recovered during the turn-off process. The value of Q_{RR} depend on the rate of fall of on-state current and the peak value of on-state current before turn-off. Q_{RR} causes corresponding energy loss within the device.

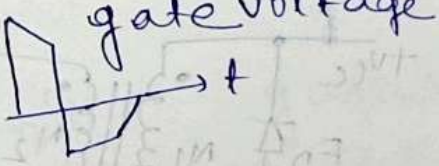
Triggering circuit

For gate triggering, a signal is applied between the gate and cathode of the device. Three types of signals can be used for this purpose. They are either dc, ac or pulse signals.

The main advantage of pulse gate triggering is that there is no need of applying continuous signals and the gate losses are very much reduced. Electrical isolation is also provided between main device supply and it's gating signals. A pulse transformer is required for isolation or an optocoupler can do isolation.

Triggering circuit with short pulse





→ ~~This type of pulse isolation is suitable for pulses of typically 50 to 100 μs.~~

Fig.-- SCR firing circuit using Pulse transformer short pulses.

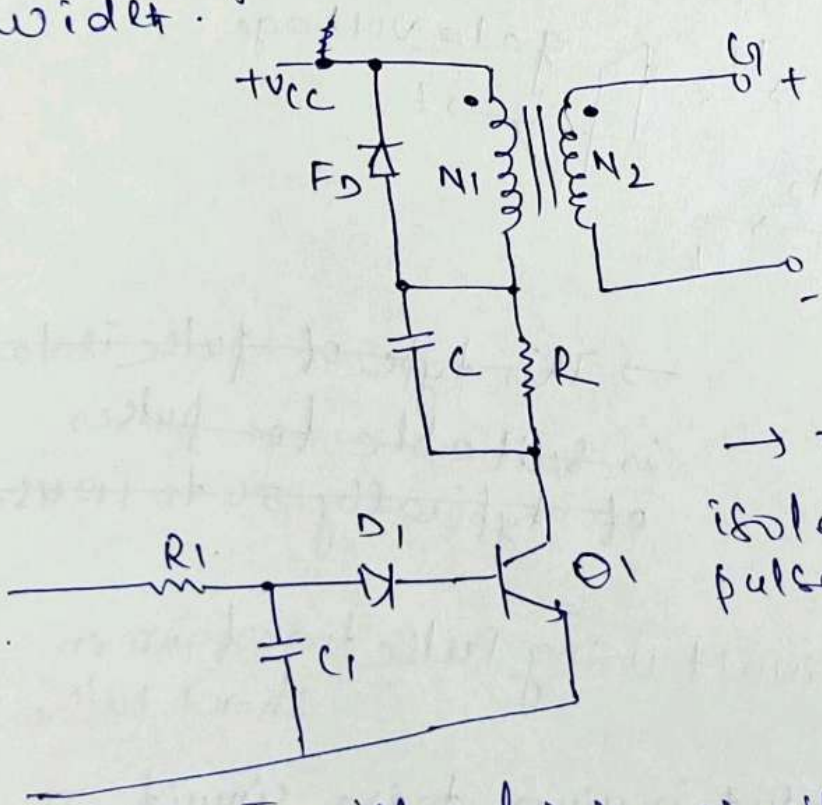
→ A Square wave input is given to the circuit. The R-L circuit converts the square wave into a pulse as shown above.

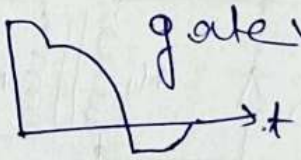
→ When this pulse is applied to the base transistor Q_1 the transistor turns on and the V_{cc} is applied to the primary winding, then voltage induced across the secondary winding, the secondary voltage act as a triggen voltage of thyristor.

→ When the pulse is removed, transistor T is off and a voltage of opposite polarity is induced across primary. The free wheeling diode F_D starts conducting and dissipates the stored energy of primary.

→ The pulse width can be made longen by connecting a capaciton C across the resistor R as shown below.

→ The transformen carries unidirectional current and the magnetic core saturate, thereby limiting the pulse width.





→ This type of pulse isolation is suitable for pulses of typically 50 to 100 μs.

Fig. - Thyristor firing circuits using pulse transformen long pulse.

Triggering circuit using Pulse train

When a thyristor converter with an inductive load, the conduction period of thyristor depends on the load power factor (P.F). In such cases, the beginning of thyristor conduction is not well defined. In this situation, it is better to trigger the thyristors continuously. But a continuous gating increases thyristor losses. Therefore it is necessary to use a pulse train for triggering.

The advantages of pulse train triggering is

(i) It increases the reliability of triggering circuit.

(ii) It reduces the losses.

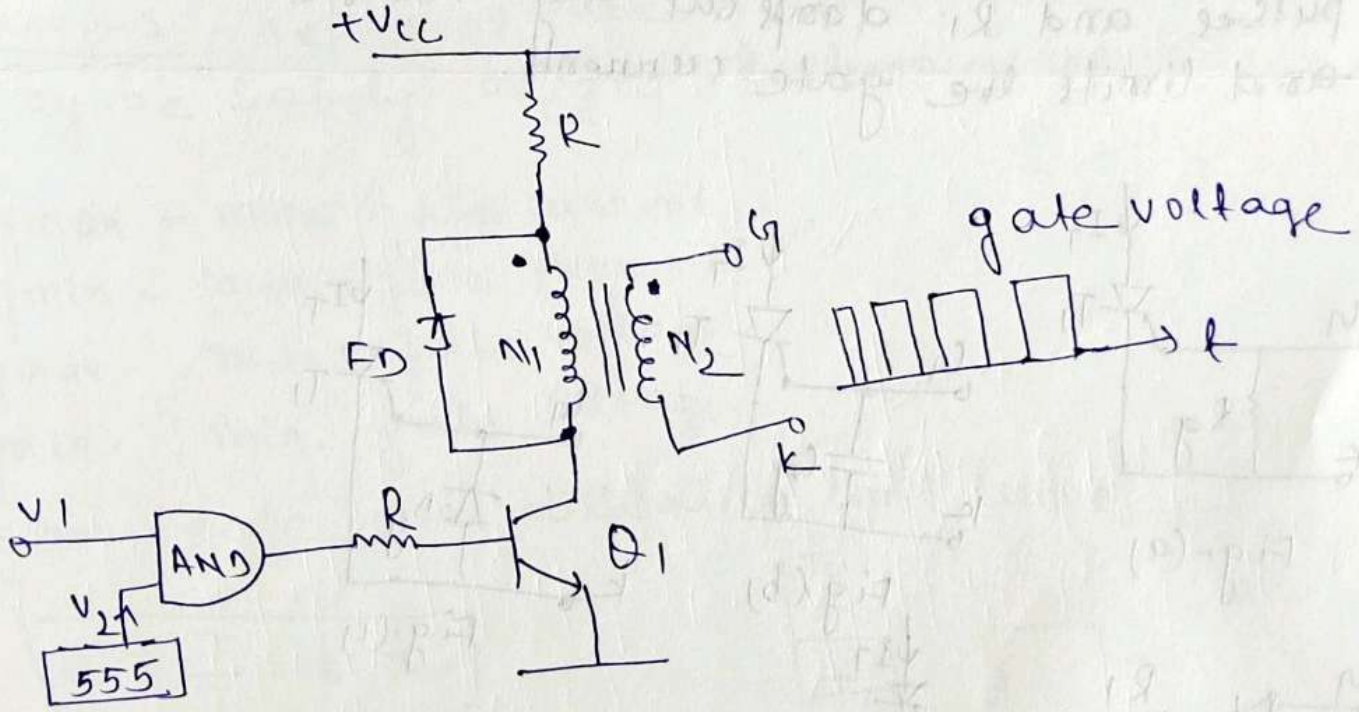


Fig.- Pulse train with timer and AND gate.

The output of gate circuit is normally between the gate and cathode along with other gate-protecting components as shown below. The resistor Rg in fig. (a) increases the $\frac{dv}{dt}$ capability of the thyristors, reduces the turn-off time and increases the holding and latching currents.

→ The capacitor Cg in fig. (b) removes high frequency noise components and increases $\frac{dv}{dt}$ capability and gate time.

→ The diode Dg in fig. (c) protects the gate from negative voltage.

→ All these features can be combined as shown in fig. (d). where D_1 allows only the positive pulses and R_1 damps out any transient oscillation and limits the gate currents.

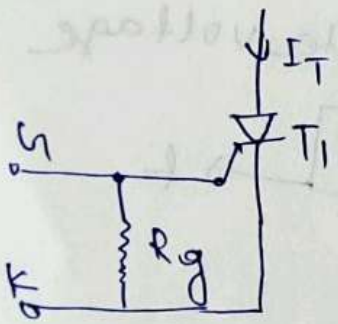


Fig-(a)

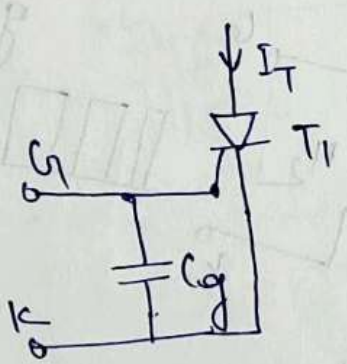


Fig (b)

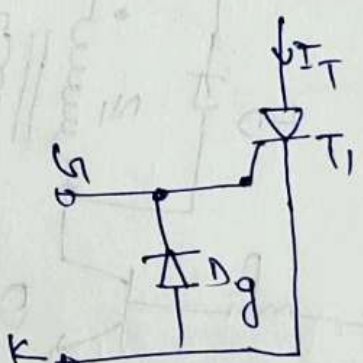


Fig.(c)

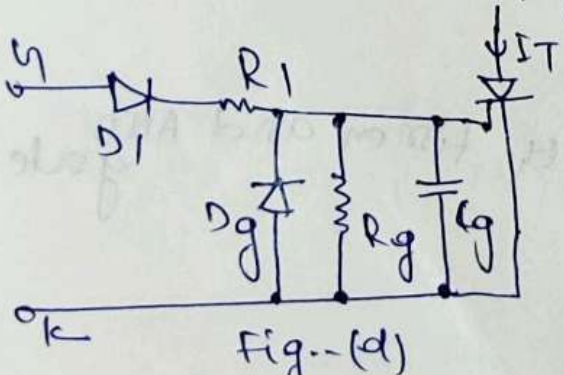
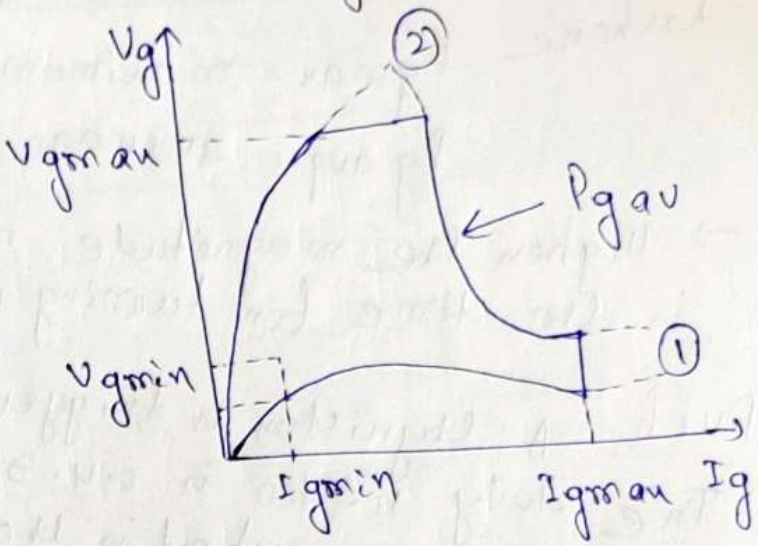


Fig.-(d)

→ The gate should be protected from triggering by a high frequency on an interference signal.

Gate characteristics

The graph between gate voltage and gate current of a thyristor is known as gate characteristics.

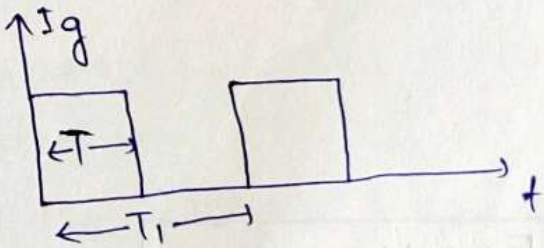


Curve-1 represent the lowest gate voltage required to turn-on the thyristor.

Curve-2 - represent the maximum gate voltage that may be safely applied to turn-on the SCR.

Igmax - max. gate current
Igmin - min. gate current
Vgmax - max. gate voltage
Vgmin - min. gate voltage.
Pg(av) - gate power dissipation limit curve.

$$\sigma = \frac{T}{T_1} = f \cdot T$$



where σ = duty cycle
T = time period.
f = frequency of firing in Hz

→ Duty cycle is defined as the ratio of pulse on period to the periodic time of pulse.

The relation between P_{gmax} & P_{gavg} is

$$P_{gmax} = \frac{P_{gavg}}{\sigma}$$

where P_{gmax} = maximum gate power
P_{gavg} = average gate power.

→ Higher the magnitude of gate current pulse, lesser is the time for turning on the thyristor.

Prob. A thyristor is triggered by a pulse train of 5kHz. The duty ratio is 0.4. If the allowable average power is 100W. what is the maximum allowable gate drive power?

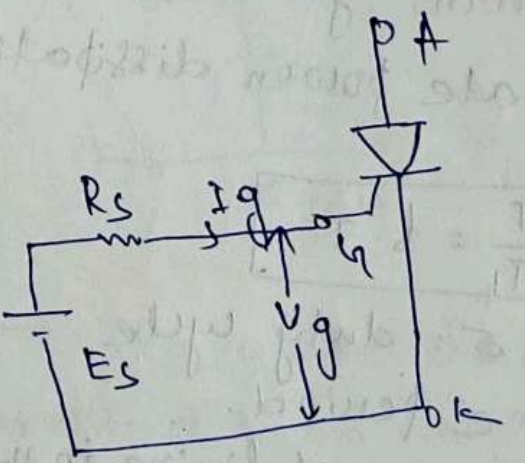
given $f = 5kHz$, $\sigma = 0.4$, $P_{gav} = 100W$

$P_{gmax} = ?$

we know $\frac{P_{gav}}{\sigma} = P_{gmax} \Rightarrow \frac{100}{.4} = P_{gmax}$

$\Rightarrow P_{gmax} = 250W$.

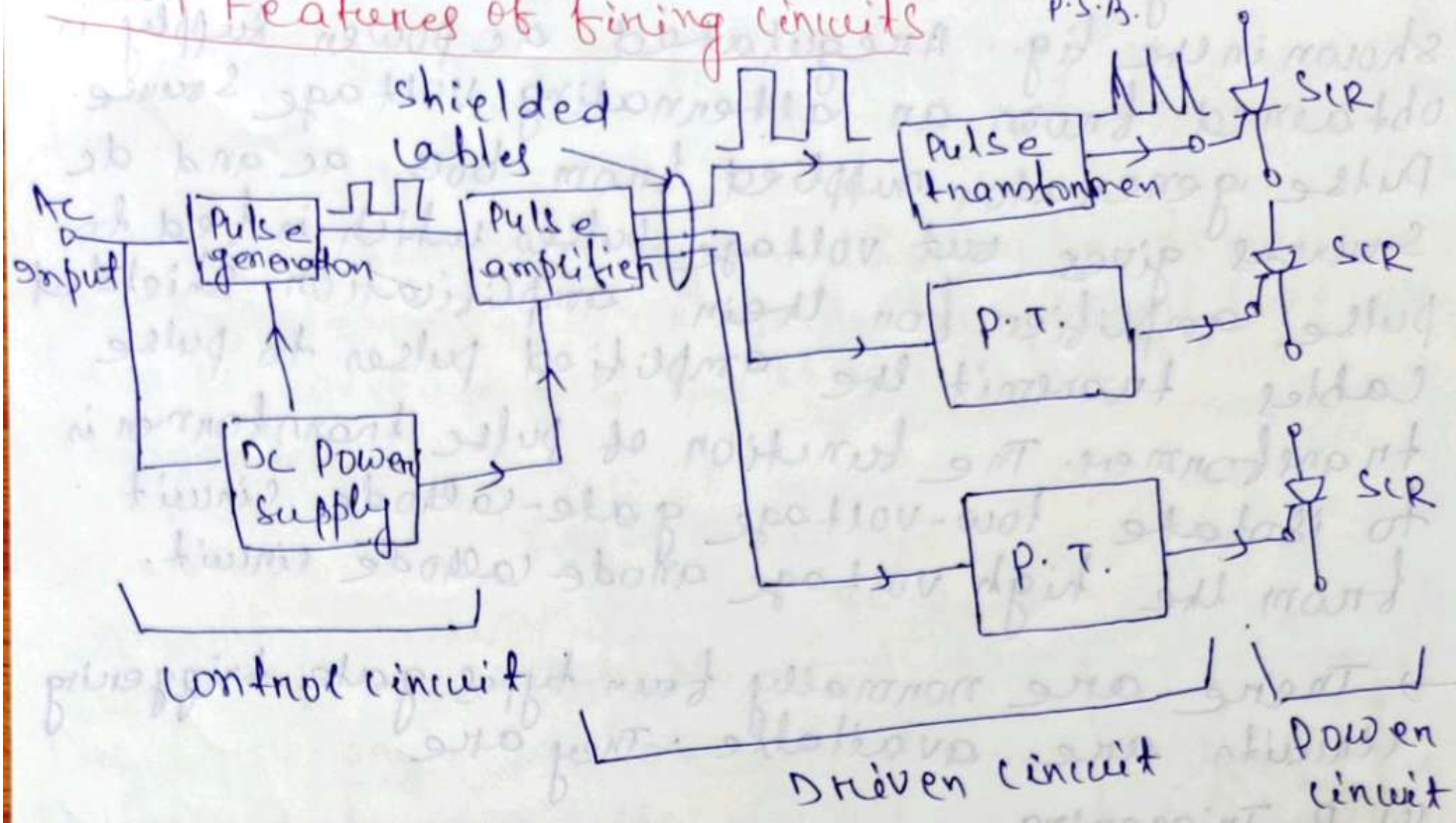
Design of gate ckt.



$$E_s = V_g + R_s I_g$$

Main Features of firing circuits

195
P.S.B.



Here P.T → Pulse transformer

A firing circuit should fulfil the following two functions

① If the power circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of power circuit. These pulses must be periodic in nature and the sequence of firing must correspond with the type of thyristorised power controller.

② The control signal generated by a firing circuit may not be able to turn on an SCR. It is therefore common to feed the voltage pulses to a driven circuit and then to gate-cathode circuit. A driven circuit consists of a pulse amplifier and a pulse transformer.

A firing circuit scheme consists of the components shown in the fig. A regulated dc power supply is obtained from an alternating voltage source. Pulse generator supplied from both ac and dc sources gives out voltage pulses which is fed to pulse amplifier for their amplification. Shielded cables transmit the amplified pulses to pulse transformers. The function of pulse transformer is to isolate low-voltage gate-cathode circuit from the high voltage anode-cathode circuit.

→ There are normally four types gate triggering circuits are available. They are

(i) R- Triggering
(ii) RC- Triggering
(iii) UJT- triggering
(iv) Cosine Law triggering.

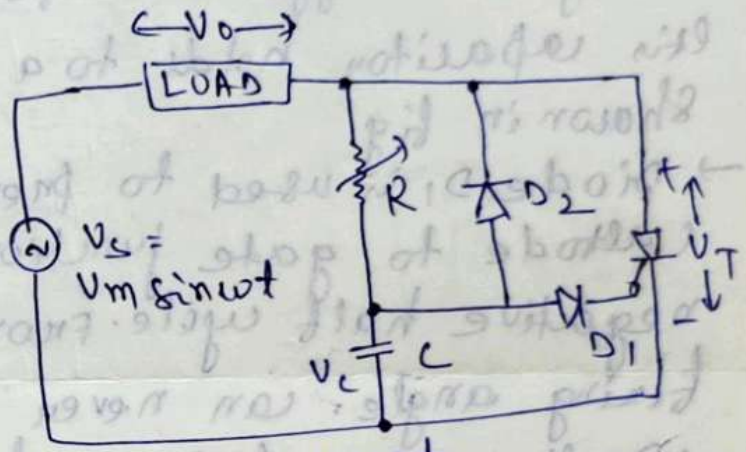
R-C Triggering

In this circuit the firing angle can be controlled from 0° to 180°.

Firing angle → A firing angle may be defined as the angle measured from the instant that gives largest average output voltage to the instant it is triggered.

R-C half-wave triggen circuit

→ By varying the resistor R', the firing angle can be controlled from 0° to 180°.



→ In the negative half-cycle, the capacitor 'C' charges through D2 with lower plate positive to the peak supply voltage Vm at ωt = -90°.

→ when

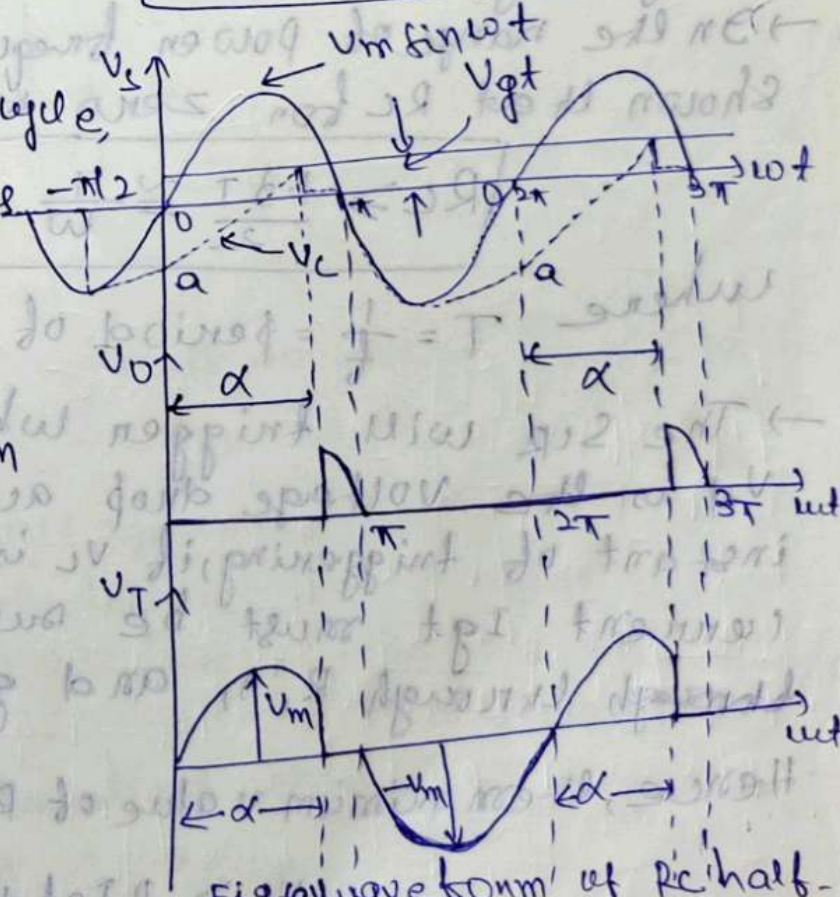


Fig (a) waveforms of RC half-wave ckt of high value of R'

→ After $\omega t = -90°$, V_s decreases from $-V_m$ at $\omega t = -90°$ to zero at $\omega t = 0°$. During this period, capacitor voltage V_c fall from $-V_m$ at $\omega t = -90°$ to some lower value $-Oa$ at $\omega t = 0°$.

→ When the SCR anode voltage passes through zero and becomes positive, C begins to charge through variable resistance R from the initial voltage $-Oa$.

→ When capacitor charges to positive voltage equal to gate triggen voltage $\underline{V_{gt}}$, SCR is fired and after this capacitor holds to a small positive voltage as shown in fig.

→ Diode D_1 is used to prevent the breakdown of cathode to gate junction through D_2 during the negative half cycle. From the fig. we observe that firing angle can never be zero and 180°.

→ In the range of power frequencies, it may be empirically shown that RC for zero output voltage is given by

$$RC \geq \frac{1.3T}{2} \cong \frac{4}{\omega} \quad \text{---(1)}$$

where $T = \frac{1}{f}$ = period of ac line frequency in second

→ The SCR will triggen when $V_c = V_{gt} + V_d$, where V_d is the voltage drop across diode D_1. At the instant of triggering, if V_c is assumed constant, the current I_{gt} must be supplied by voltage source through R, D_1 and gate to cathode circuit.

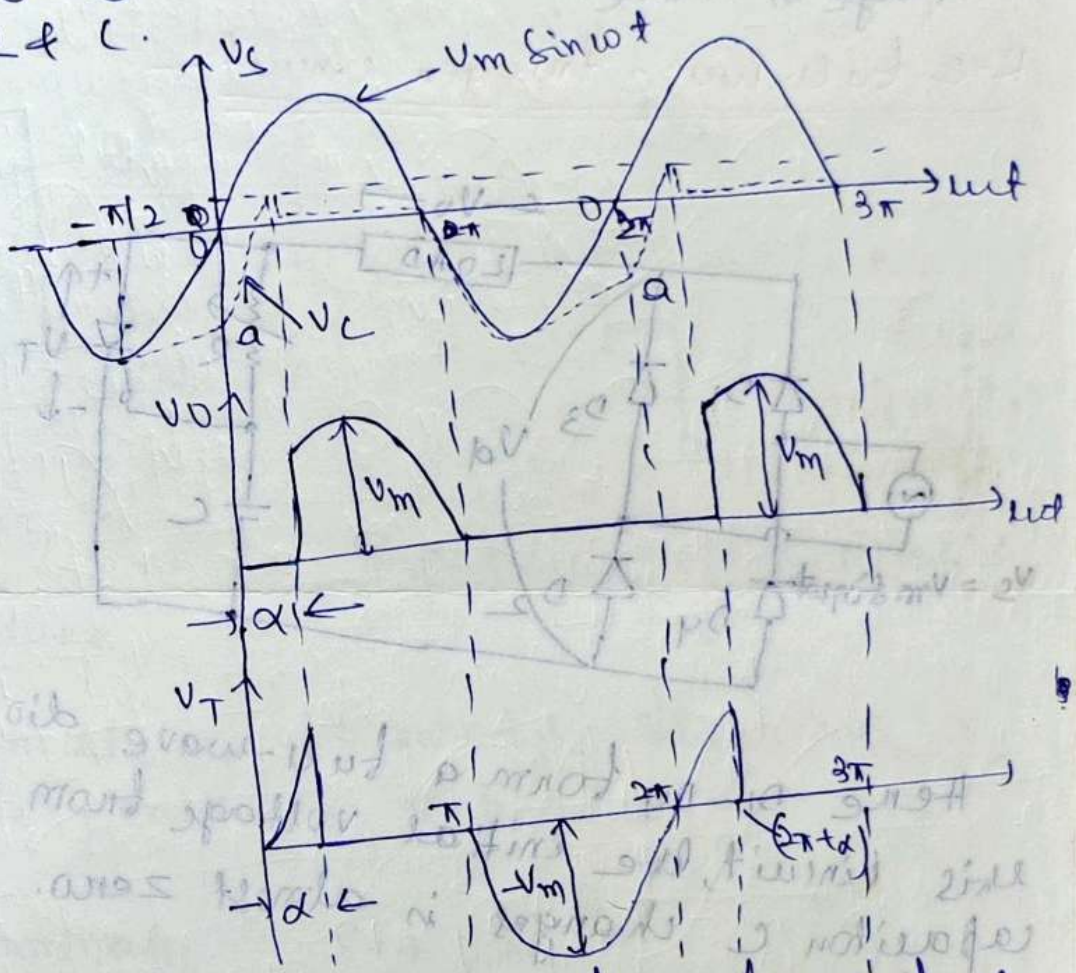
Hence, the maximum value of R is given by

$$V_s \geq R I_{gt} + V_c$$

$$V_s \geq R I_{gt} + V_{gt} + V_d$$

$$R \leq \frac{V_s - V_{gt} - V_d}{I_{gt}} \quad \text{---} (2)$$

From eqn (1) & (2) we can calculate approximate values of R & C.

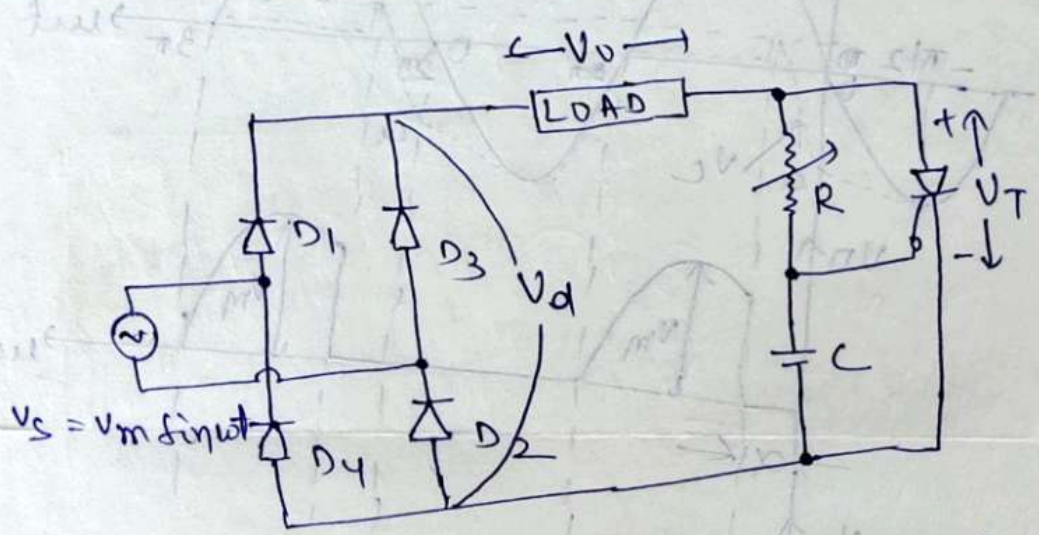


Fig(b) waveform for RC half-wave ckt of low value of R.

→ When SCR triggers, voltage drop across it falls to 1 to 1.5 V. This in turn, lowers the voltage across R and C to this low value of 1 to 1.5 V. Low voltage across SCR during conduction period keeps C discharged in positive half cycle until negative voltage cycle across C appears.

In fig. (a) - R is more, less current will flow so the time taken for C to change from $-\sigma a$ to $(V_{gt} + V_d) \cong V_{gt}$ is more, firing angle is more and therefore average output voltage is low. In fig. (b) R is less, firing angle is low and average output voltage is more.

R-C full-wave triggen circuit -



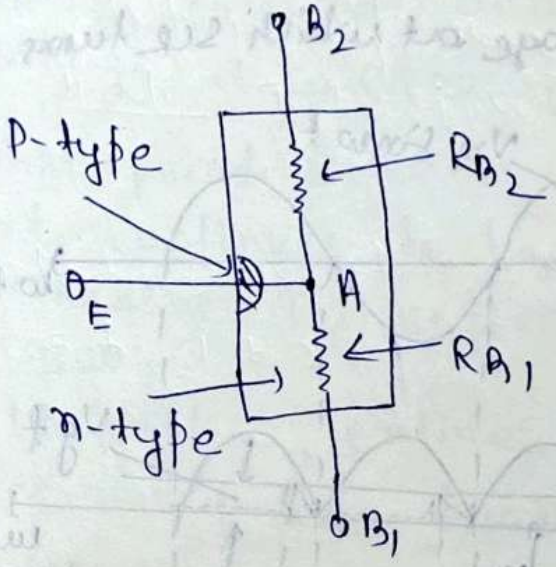
Here $D_1 - D_4$ form a full-wave diode bridge in this circuit, the initial voltage from which the capaciton C changes is almost zero.

→ When capaciton changes to a voltage equal to V_{gt}, SCR triggers and rectified voltage V_d appears across load as V_o.

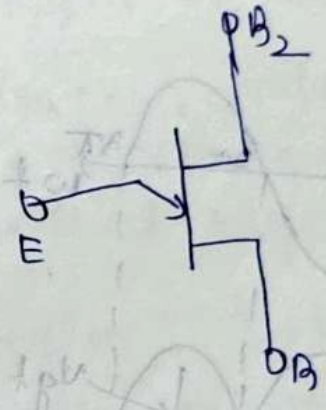
→ The value of RC is calculated by the empirical relation $\boxed{RC \geq 50 \frac{T}{2} \cong \frac{157}{\omega}}$

Unijunction Transistor.

R and RC triggering circuits gives prolonged pulses. Therefore power dissipation in the gate circuit is large. Therefore RC triggering can't be used for automatic or feedback control system. These difficulties are overcome by the use of UJT triggering ckt.



Basic structure

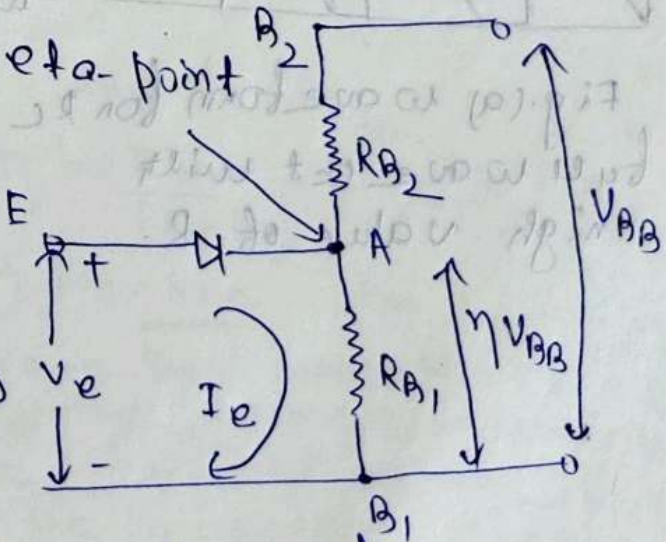


Symbolic representation

An UJT is made up of an n-type silicon base to which P-type emitter is embedded.

→ It has 3 terminals, the emitter E, base-one B_1 and base-two B_2.

eta-point



Equivalent ckt

→ Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. ~~The resistance~~ is the interbase resistance R_{BB}.

The value of R is given by

$$V_s \geq R I_{gt} + V_c$$

$$\text{or } V_s \geq R I_{gt} + V_{gt} + V_d$$

$$\text{or } \boxed{R \leq \frac{V_s - V_{gt}}{I_{gt}}}$$

where V_s is the source voltage at which SCR turns ON.

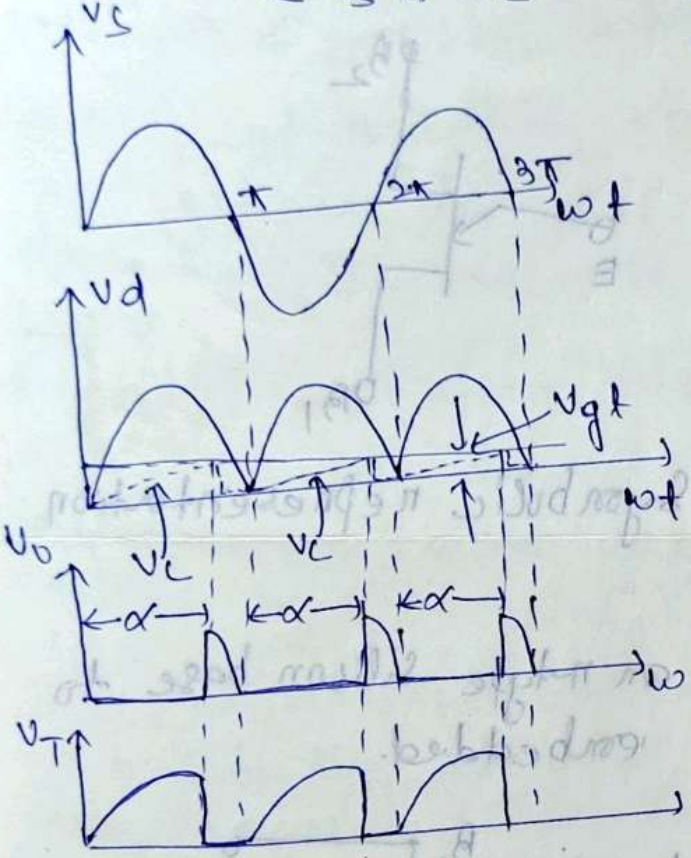


Fig.(a) waveform for RC half wave ckt with high value of R.

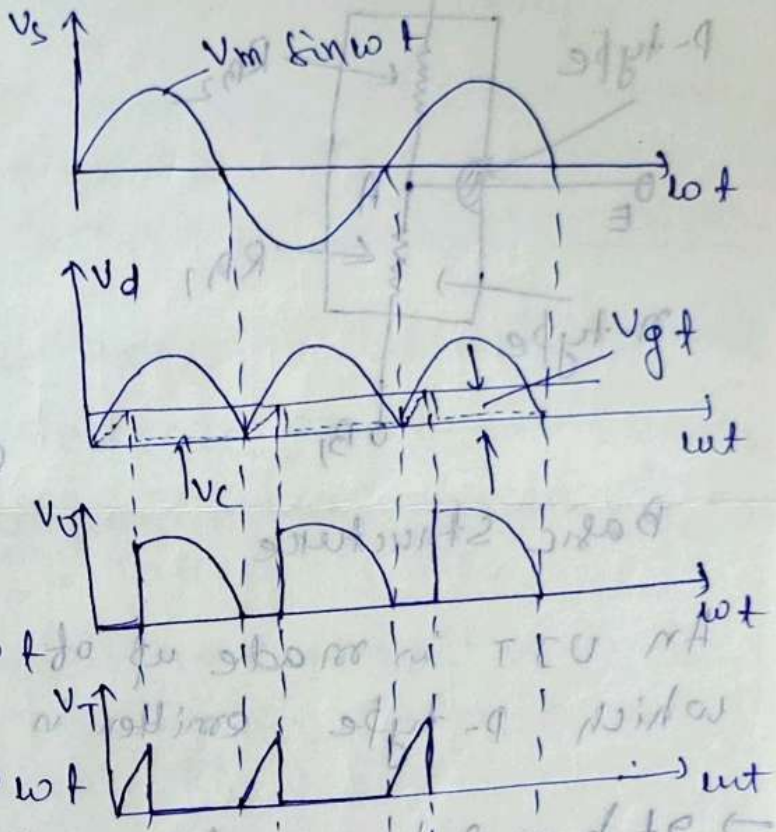


Fig-(b) - For low value of R.

as shown by the curve PS. When voltage V_e is equal to $\eta V_{BB} + V_D$ at point B, I_e is +ve and E-B_1 junction begins to conduct. Here V_D is the forward voltage drop of E-B_1 junction.

→ Point B is called peak point and the corresponding emitter potential and current are V_p (peak-point voltage) & I_p (peak-point current respectively.

→ At point B when $V_e = \eta V_{BB} + V_D$, conduction starts. It continues from B to C. I_e increases and V_e decreases. This region BC is called negative resistance region.

→ At point C, entire base region is saturated and resistance R_{B1} does not decrease any more. After then increase in I_e is accompanied by a rise in voltage V_e. This is CQ. Point 'C' is called valley point.

Prob. The intrinsic stand-off ration for an UJT is 0.6. If the interbase resistance is 10 kΩ, what are the values of R_{B1} and R_{B2}?

Soln. $R_{BB} = 10\text{k}\Omega$, $\eta = 0.6$ $R_{BB} = R_{B1} + R_{B2}$

$\therefore 10 = R_{B1} + R_{B2}$, $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} \Rightarrow 0.6 = \frac{R_{B1}}{10}$

$\Rightarrow R_{B1} = 6\text{k}\Omega$, $\therefore R_{B2} = 10 - 6 = 4\text{k}\Omega$.

Prob. An UJT has 10V between the bases. If the intrinsic stand off ratio is .65, find the value of stand off voltage, what will be the peak-point voltage if the forward voltage drop in the pn junction .7V.)

Ans $V_{BB} = 10V$, $\eta = .65$, $V_D = .7V$

Stand off voltage $\eta V_{BB} = .65 \times 10 = 6.5\,V$

$V_p = \eta V_{BB} + V_D = 6.5 + .7 = 7.2\,V$.

→ R_{B_1} and R_{B_2} are the internal resistances from bases B_1 and B_2 to emitter point A.

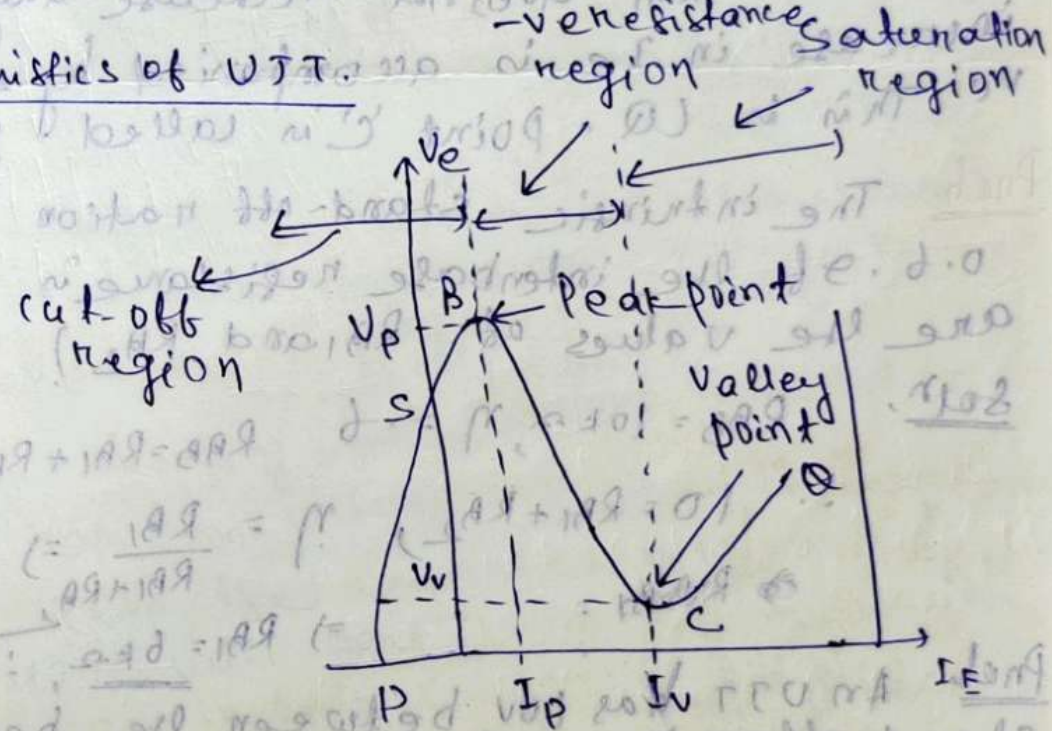
→ When a voltage V_{BB} is applied across the two base terminals B_1 & B_2, the potential of A w.r.t. B_1 or voltage drop across AB_1 is given by

$$V_{AB_1} = \frac{V_{BB}}{R_{B_1}+R_{B_2}} \cdot R_{B_1} = \frac{R_{B_1}}{R_{B_1}+R_{B_2}} \cdot V_{BB} = \eta V_{BB}$$

where $\eta = \frac{R_{B_1}}{R_{B_1}+R_{B_2}}$ is called the intrinsic stand-off ratio. Typical values of η are .51 to .82.

Interbase resistance $R_{BB} = R_{B_1} + R_{B_2}$ is of the order of 5 to 10 kΩ.

V-I characteristics of UJT:



Let a voltage V_e be applied between emitter E and base B_1 so that at E is +ve w.r.t. B_1. Let this voltage be increased from zero. As long as the emitter voltage $V_e < \eta V_{BB}$, the E-B_1 unijunction is reverse biased & emitter current is -ve

UJT Oscillaton Triggering.

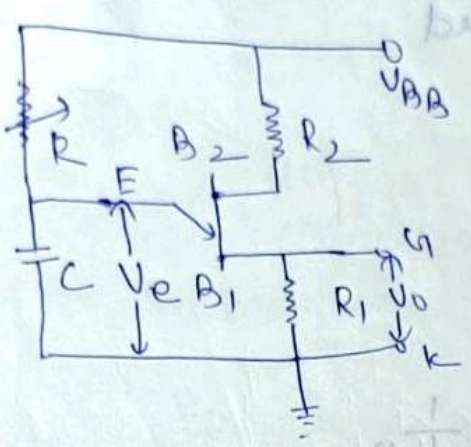


Fig a - UJT Oscillaton connection diagram

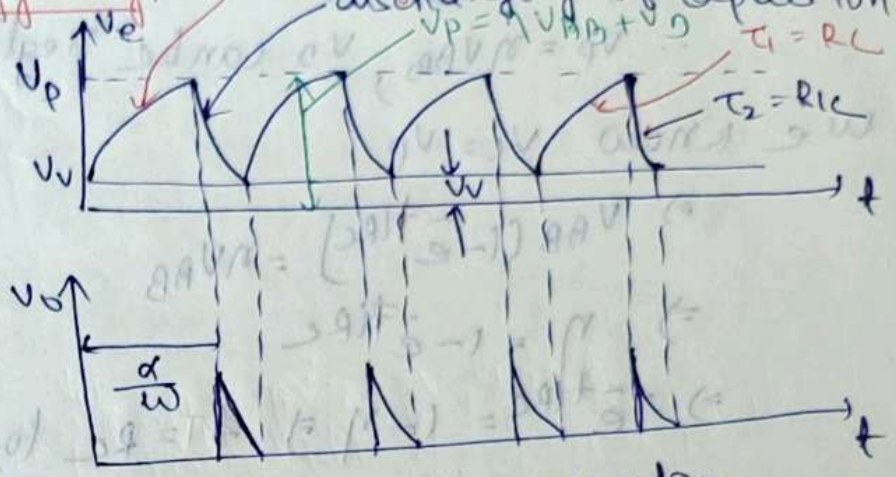


Fig-(b) UJT Oscillaton voltage waveform.

Assuming that capaciton is initially unchanged. when V_{BB} is applied, current will flow in the circuit in path V_{BB}-R-C-gd (due to UJT off). So capaciton will get changed with upper plate positive. During the charging period, the voltage across the capaciton V_c rises in the exponential manner until it reaches the peak point voltage V_p.

$$V_c = V_e = V_{BB}(1 - e^{-t/(RC)})$$

where RC = charging time constant of R-C ckt = T_1.

The increasing capaciton voltage is shown in the wave-form in fig. when $V_c = V_p$, the unijunction between E-B_1 Breaks down, UJT will start conducting. So capaciton start to discharge in path C-UJT-R_1-gd. Discharging voltage will appear across R_1 which is shown as a triggering pulse waveform.

The discharge of the capaciton occurs when V_c is equal to V_p. (peak-point voltage)

$V_p = \eta V_{BB} + V_D$

$\therefore V_p = \eta V_{BB}$, V_D can be neglected

We know $V_c = V_p$

$\Rightarrow V_{BB}(1 - e^{-t/RC}) = \eta V_{BB}$

$\Rightarrow \eta = 1 - e^{-t/RC}$

$\Rightarrow e^{-t/RC} = 1 - \eta \Rightarrow t = RC \log_e \frac{1}{1-\eta}$

$\Rightarrow \boxed{t = 2.3\, RC \log_{10} \frac{1}{1-\eta}}$

$\therefore \boxed{T = RC \ln \frac{1}{1-\eta}}$

The frequency of oscillation $= f = \frac{1}{T}$

→ The value of $\boxed{R_2 = \frac{10^4}{\eta V_{BB}}}$

The max. value of R

$$R_{max} = \frac{V_{BB} - V_p}{I_P} = \frac{V_{BB} - (\eta V_{BB} + V_D)}{I_P}$$

$$R_{min} = \frac{V_{BB} - V_v}{I_V}$$

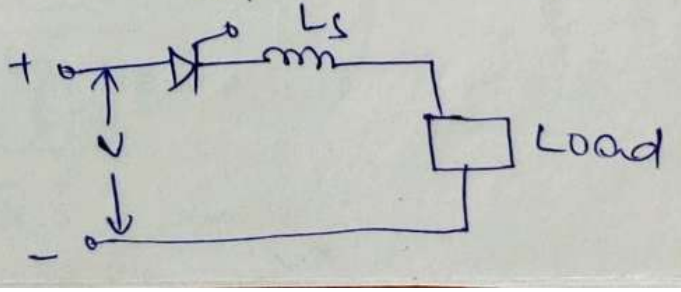
∴ width of triggering pulse

$$\boxed{t_g = R_{B1} C}$$

Thyristor Protection.

Reliable operation of a thyristor demands that that it's specified ratings should not be exceeded. In practice, a thyristor maybe subjected to overvoltage or overcurrents. During SCR turn-on, $\frac{di}{dt}$ may be large. There maybe false triggering of SCR by high value of $\frac{dv}{dt}$. A spurious signal across gate-cathode terminals may lead to unwanted turn-on. A thyristor must be protected all such abnormal conditions for satisfactory and reliable operation of SCR circuits and the equipments. SCRs are very delicate devices, their protection against abnormal operating conditions is essential.

(a) $\frac{di}{dt}$ protection. → When thyristor is forward biased & is turned on by a gate pulse, conduction of anode current spreads across the whole area of junction. If the rate of rise of anode current i.e. $\frac{di}{dt}$ is large as compared to spread velocity of carriers, local hot spots will be created near the gate connection on account of high current density. This heating may destroy the thyristor. So the value of $\frac{di}{dt}$ should be below acceptable limit by using small inductor called $\frac{di}{dt}$ inductor in series with the circuit. Typical $\frac{di}{dt}$ limit value of SCR are 20-500 A/μsec.



$\frac{dv}{dt}$ protection.

With forward voltage across the anode and cathode of thyristor, the two outer junctions are forward biased but the inner junction J_2 is reverse biased. This reverse biased junction J_2 acts as a capacitor due to charges existing across the junction.

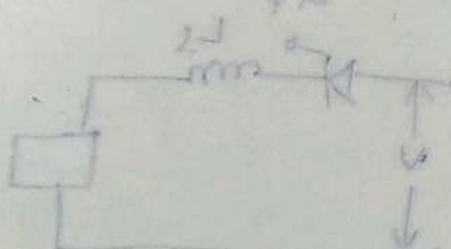
If the entire anode to cathode forward voltage 'Va' appears across J_2 junction & the charge is denoted by Q, then charging current 'i' is given by

$$i = \frac{dQ}{dt} = \frac{d(C_j \cdot V_a)}{dt} = C_j \frac{dV_a}{dt} + V_a \frac{dC_j}{dt}$$

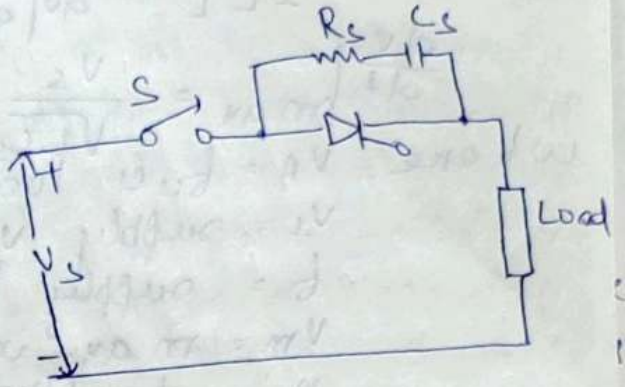
$$\Rightarrow i = C_j \frac{dV_a}{dt} \quad \text{as } C_j \text{ is constant.}$$

If the rate of rise of forward voltage $\frac{dV_a}{dt}$ is more, the charging current 'i' will be more. This charging current plays the role of gate current & turns on the SCR even without gate signal is applied. This is called mal operation of SCR. It is also called $\frac{dv}{dt}$ turn on.

For controllable operation of thyristor $\frac{dv}{dt}$ must be kept below the rated limit. Typical values of $\frac{dv}{dt}$ are 20-500 V/μsec. The false turn-on of a thyristor by large $\frac{dv}{dt}$ can be prevented by using a snubber ckt in parallel with the device.



Snubben circuit.



A snubben circuit consists of a series combination of Rs and Cs in parallel with the thyristor as shown in fig.

→ The capacitor Cs in parallel with the device is sufficient to prevent unwanted $\frac{dv}{dt}$ triggering of the SCR.

→ when switch 'S' is closed, a ~~sud~~ sudden voltage appears across the circuit, capacitor Cs behaves like short circuit, therefore voltage across SCR is zero. Voltage across capacitor will also appear across the thyristor. So $\frac{dv}{dt}$ is less which is under $\frac{dv}{dt}$ triggering of thyristor.

→ Before SCR is triggered by a gate pulse, Cs charges to full voltage Vs. when SCR is turned on, capacitor is discharged through the SCR and sends a current equal to Vs/(resistance of Cs + Resistance of SCR).

As this resistance is low, the turn on $\frac{di}{dt}$ will tends to be very high, as a result, SCR may be destroyed.

→ In order to limit the magnitude of discharge current, a resistance Rs is inserted in series with the Cs.

Design of Snubben circuit.

$$C_s = \frac{10 VA}{V_s^2} \times \frac{60}{f} \mu F$$

$$R_s = 2\eta \sqrt{\frac{L}{C_s}}$$

$$C_S = \frac{1}{2L}\left[\frac{.564 V_m}{dv/dt}\right]^2$$

$$\left.\frac{dv}{dt}\right|_{max} = \frac{V_s}{\sqrt{LC_s}}$$

where V_A = full load power rating of the device in watts
V_s = supply voltage
f = supply frequency
V_m = max. input voltage
η = damping ratio = .65

Prob Design a snubber circuit to provide reliable $\frac{dv}{dt}$ protection to a SCR. The SCR have a maximum $\frac{dv}{dt}$ capability of 40V/μs. The input line to line voltage has a peak value of 325V and line inductance is .1mH.

Soln.

$$C_S = \frac{1}{2L}\left[\frac{.564 V_m}{dv/dt}\right]^2$$

$$= \frac{1}{2\times .1\times 10^{-3}}\left[\frac{.564\times 325}{40/10^{-6}}\right]^2 = .105\,\mu F$$

$$R_S = 2\eta\sqrt{\frac{L}{C_S}} \qquad \eta = .65$$

$$= 40.31\,\Omega$$

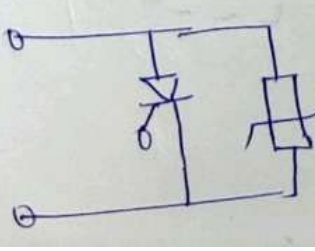
Overvoltage protection.

A thyristor may be subjected to overvoltage due to bad commutation, short circuit, transients due to switching operation, lightning strokes & so on. Overvoltage transients are the main cause of SCR failure. Transient overvoltages cause either maloperation of the circuit by unwanted turn on of a SCR or permanent damage to the device due to reverse breakdown. A thyristor may be subjected to internal or external overvoltages.

Internal overvoltage. During commutation of a SCR, large voltages are generated internally. As this internal voltages are several times of the breakover voltage of the device, the thyristor may be destroyed permanently.

External overvoltages External overvoltages are caused due to lightning strokes on the lines feeding the thyristor system and due to the interruption of current flow in an inductive ckt. Such overvoltages may cause turn-on of a thyristor. overvoltages may damage the thyristor by an inverse breakdown. For reliable operation, the overvoltages must be suppressed.

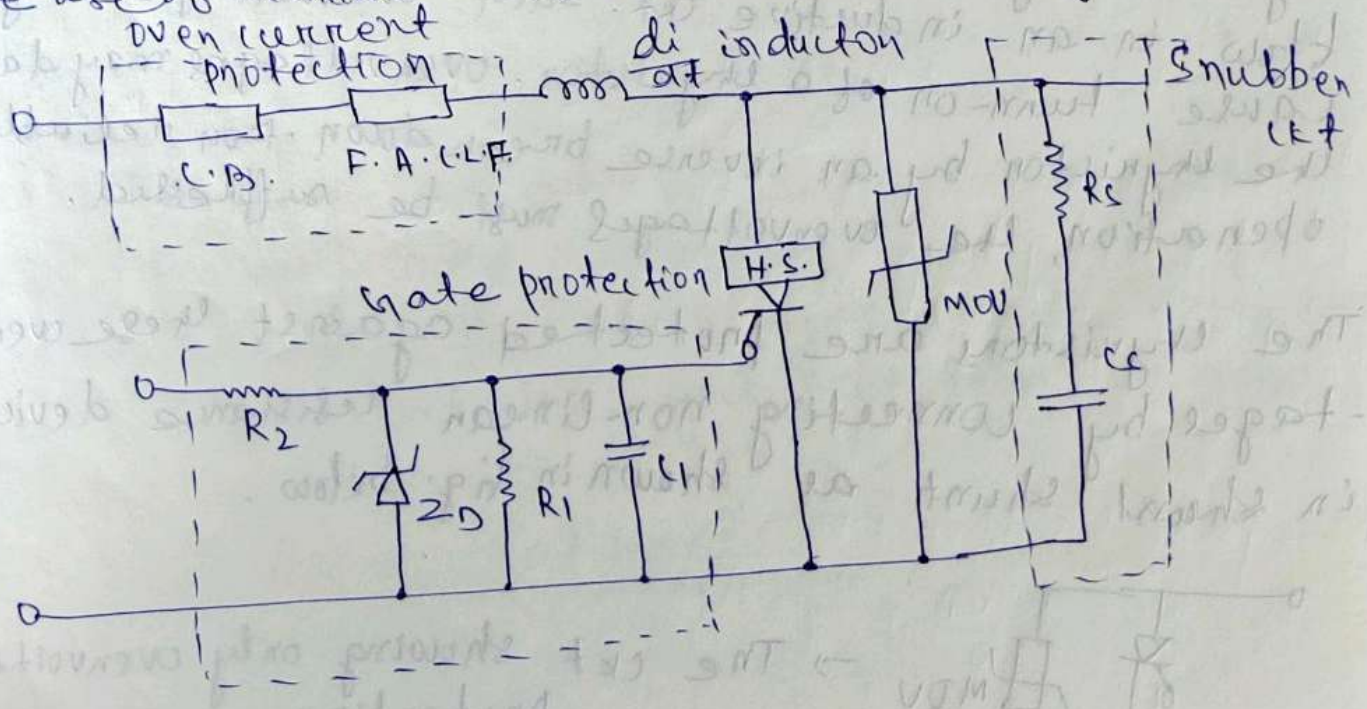
The thyristors are protected against these overvoltages by connecting non-linear resistance devices in shunt as shown in fig. below.



→ The ckt showing only overvoltage protection.

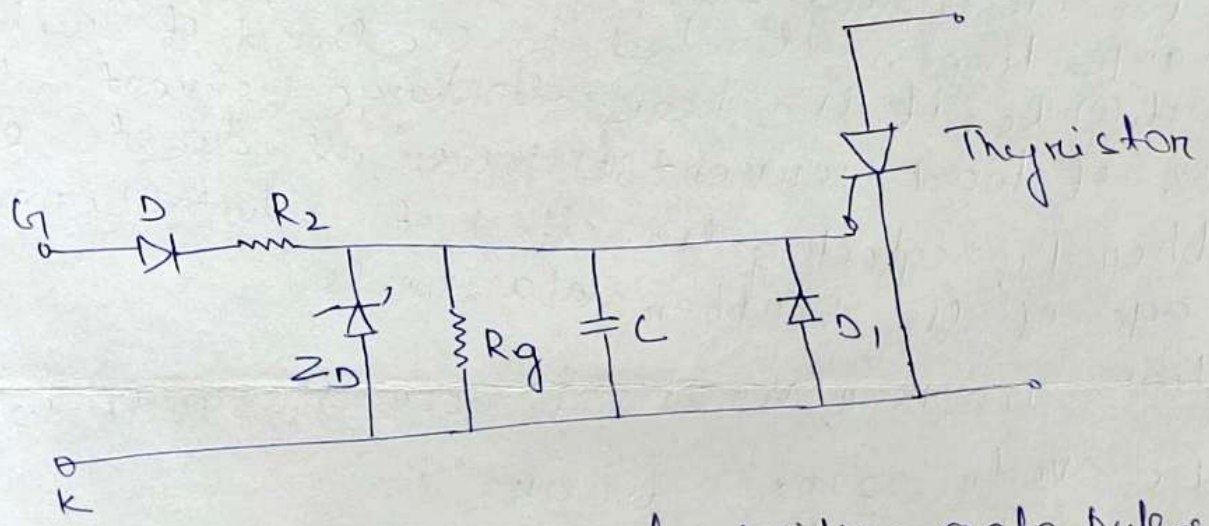
The protective device has falling resistance characteristics with increasing voltage. Under normal working condition, the device has a high resistance and draws only a small leakage current. When a voltage surge appears, the device operates in low resistance region and produces a virtual short circuit across the SCR and protect from high voltages. The commonly used non-linear devices are metal oxide varistors (MOV) and selinium thyriston diodes. After the surge energy is dissipated in the non-linear resistor, the device returns to its high resistance region.

Overcurrent protection. Generally thyristons have small thermal time constant. If a thyriston is subjected to overcurrent due to faults, short circuit occurs, it's junction temperature may exceed the rated value & the device may be damaged. For this overcurrent protection of SCR is required. Overcurrent protection in SCR ckt is achieved through the use of circuit breakers and fast-acting-fuses.



Gate protection.

Overvoltage across the gate ckt. can cause false triggering of the SCR. overcurrent may raise junction temperature beyond specified limit leading its damage. Protection against over-voltage is achieved by connecting a zener diode (Z_D) across the gate ckt. A resistor R_2 connected in series with the gate ckt provides protection against overcurrent.



→ The diode D allows only positive gate pulses. The resistance Rg increases the $\frac{dv}{dt}$ capability of the SCR, reduces the turn-off time and increases the holding and latching current. The capacitance C removes high frequency noise components from gate signal and increases $\frac{dv}{dt}$ capability and gate delay time. Diode D_1 protect the gate ckt from -ve gate voltage.

$\frac{di}{dt}$ and $\frac{dv}{dt}$ Limitations.

$$L_s = \frac{V_s t_r}{I_L} \quad \text{——(1)}$$

$$C_s = \frac{I_L t_f}{V_s} \quad \text{——(2)}$$

Phase controlled Rectifier

The phase-controlled rectifiers convert fixed Ac voltage to a variable dc voltage. As these rectifiers employ line commutation or natural commutation, these are also known as line commutated converters or natural commutated converters.

→ Diode Rectifiers provide a fixed o/p voltage only. To obtain controlled o/p voltages, phase-control thyristors are used instead of diodes. The o/p voltage of thyristor rectifiers is varied by controlling the delay or firing angle of thyristors.

→ These phase-controlled rectifiers are simple and less expensive and the efficiency of these rectifiers is above 95%. Since these rectifiers convert ac to dc, these controlled rectifiers are also called ac-dc converters and are extensively used in industries (variable speed drives) where controlled dc power is required.

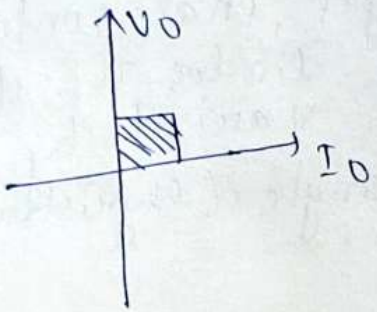
→ The phase-control converters can be classified into two types depending on the input supply (1) single-phase converters (2) three-phase converters. Each type can be subdivided into (a) Semi converter (b) Full-converter and (c) dual converter.

→ A Semi-converter is a one-quadrant converter and it has one polarity of o/p voltage and current.

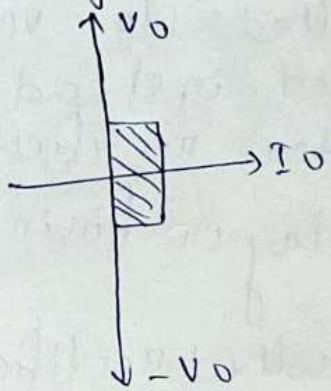
→ A full-converter is a two-quadrant converter.

A two-quadrant converter is one in which o/p voltage Polarity can reverse but current direction can't reverse because of unidirectional nature of thyristors. i.e. polarity of o/p voltage can either +ve or -ve, but o/p current of full converter has one polarity only.

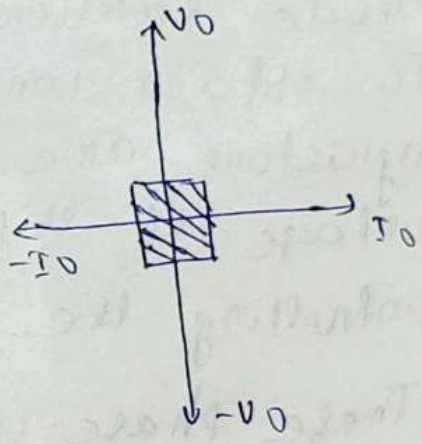
→ A dual converter can operate in four quadrants and both the o/p voltage and current can be either positive or negative.



One-quadrant converter



Two-quadrant converter



Four-quadrant converter.

Application of phase-controlled rectifier.

1. Traction systems working on dc
2. Paper mills, steel-rolling mills, printing presses and textile mills employing dc motor drives.
3. HVDC transmission system.
4. Electrochemical and electrometallurgical processes.
5. Electro-plating and Battery charging.
6. Magnetic power supplies.

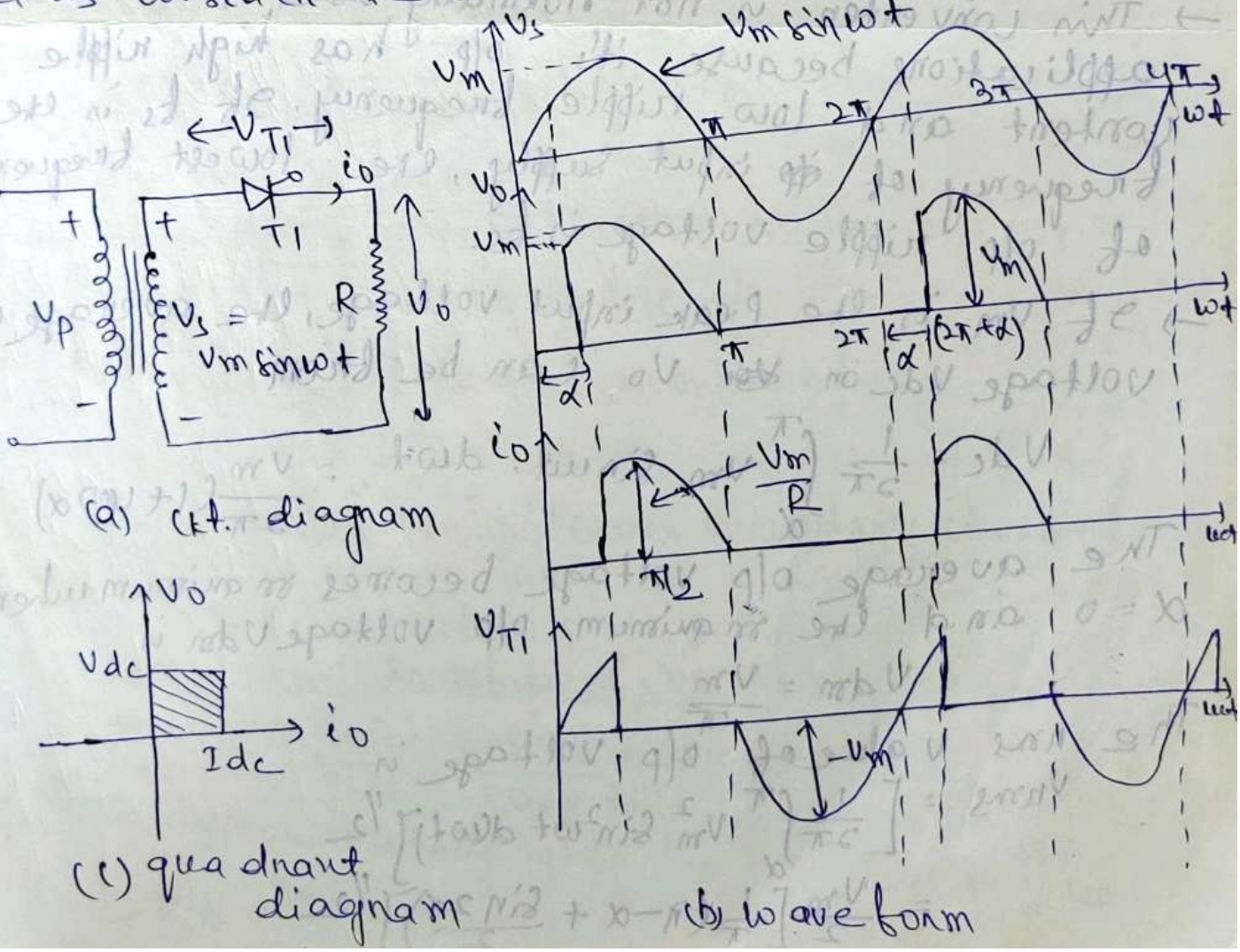
Dual converter. – Two full converters are connected back to back to the load ckt.

Principle of Phase-controlled converter operation

By varying the firing angle(α), we can control the turning on of the thyristor. Such a method of control is called as Phase-angle control. This phase angle control is a highly efficient means of controlling the average power to loads.

→ The firing angle(α) or delay angle may be defined as the angle measured from the instant that gives largest average o/p voltage to the instant it is triggered. A firing angle may be defined as the angle between the instant thyristor would conduct if it were a diode and the instant it is triggered

Let us consider the ckt with a resistive load.



During the +ve half-cycle of input voltage, the SCR anode is +ve w.r.t. cathode and the SCR is said to be forward biased. When thyristor T_1 is fired at $\omega t = \alpha$, thyristor T_1 conducts and the input voltage appears across the load.
When the input voltage starts to be -ve at $\omega t = \pi$, the thyristor anode is -ve w.r.t. cathode and the thyristor T_1 is said to be reverse biased and it is turned off. The time after the input voltage starts to go +ve until the thyristor is fired at $\omega t = \alpha$ is called the delay or firing angle α.

→ Figure 'c' shows the region of converter operation, where the o/p voltage and current have one polarity.

→ This converter is not normally used in industrial applications because its o/p has high ripple content and low ripple frequency. If f_s is the frequency of ~~the~~ input supply, the lowest frequency of o/p ripple voltage is f_s.

→ If V_m is the peak input voltage, the average o/p voltage V_{dc} or V_o can be from

$$V_{dc} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \cdot d\omega t = \frac{V_m}{2\pi}(1+\cos\alpha)$$

The average o/p voltage becomes maximum when $\alpha = 0$ and the maximum o/p voltage V_{dm} is

$$V_{dm} = \frac{V_m}{\pi}$$

The rms value of o/p voltage is

$$V_{rms} = \left[\frac{1}{2\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{2}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

Prob. For a 1-ϕ half-wave converter purely resistive load of R and $\alpha = \pi/2$, determine (a) the rectification efficiency (b) the FF (c) the RF (d) the TUF and (e) the PIV of thyristor T_1.

Soln. Given $\alpha = \pi/2$,

$$V_{dc} = \frac{V_m}{2\pi}(1+\cos\alpha) = .1592 V_m$$

$$I_{dc} = .1592 V_m / R$$

$$V_{rms} = \frac{V_m}{2}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

$$= .3536 V_m$$

$$I_{rms} = .3536 V_m / R$$

$$P_{dc} = V_{dc} \cdot I_{dc} = (.1592 V_m)^2 / R$$

$$P_{ac} = V_{rms} \cdot I_{rms} = (.3536 V_m)^2 / R$$

(a) $$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(.1592 V_m)^2}{(.3536 V_m)^2} = 20.27\%$$

(b) $$FF = \frac{V_{rms}}{V_{dc}} = \frac{.3536 V_m}{.1592 V_m} = 2.221 \text{ or } 222.1\%$$

(c) $$RF = \sqrt{FF^2 - 1} = 1.983 \text{ or } 198.3\%$$

(d) Rms voltage of transformer secondary

$$V_s = \frac{V_m}{\sqrt{2}} = .707 V_m$$

Rms value of transformer secondary current is the same as that of the load

$$I_s = .3536 V_m / R$$

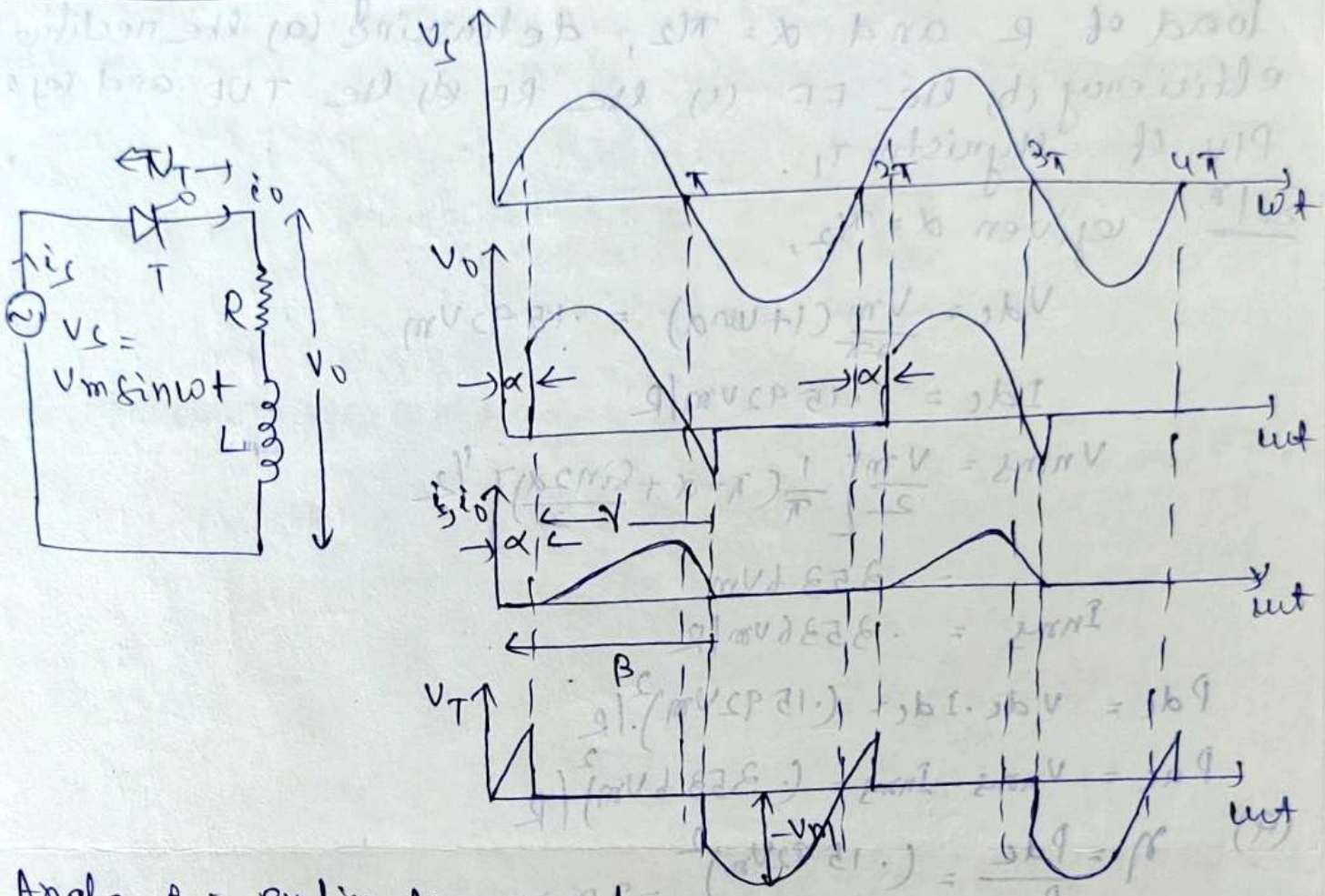
VA of the transformer $VA = V_s I_s = .707 V_m \times .3536 \frac{V_m}{R}$

$$\therefore TUF = \frac{P_{dc}}{V_s I_s} = \frac{.1592^2}{.707 \times .3536} = .1014 \quad \& \quad \frac{1}{TUF} = 9.86$$

PF is approximately equal to TUF. Thus PF = .1014

(e) The PIV = V_m

1-φ Half-wave ckt with R-L load.



Angle β = extinction angle

$(\beta - \alpha) = \gamma$ = conduction angle

At $\omega t = \alpha$, thyristor is turn on by a gate signal. Due to inductive load, current i_o rises gradually. After some time, i_o reaches maximum value & then begins to decrease. At $\omega t = \pi$, V_o is zero but i_o is not zero because of the load inductance. After $\omega t = \pi$, SCR is subjected to reverse anode voltage but it will not be turned off as load current i_o is not less than holding current. At some angle $\beta > \pi$, i_o reduces to zero & SCR is turned off as it is already reverse biased. After $\omega t = \beta$, $V_o = 0$ & $i_o = 0$.

At $\omega t = 2\pi + \alpha$, SCR is triggered again, the above cycle repeats. Hence the effect of the inductive load is increase in the conduction period of SCR.

→ Thyristor is reverse biased at $\omega t = \beta$ to 2π. Thus the ckt turn-off time $t_c = \frac{2\pi - \beta}{\omega}$ sec.

$$\therefore t_c = \frac{2\pi - (\pi + \alpha)}{\omega} \text{ sec.}$$

Average O/p voltage

$$V_o = \frac{1}{2\pi} \int_{\alpha}^{\beta} V_m \sin \omega t \cdot d(\omega t)$$

$$= \frac{V_m}{2\pi} (\cos\alpha - \cos\beta)$$

Average O/p current

$$I_o = \frac{V_m}{2\pi R} (\cos\alpha - \cos\beta) = \frac{V_o}{R}$$

$$V_{rms} = \left[\frac{1}{2\pi} \int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \cdot d\omega t \right]^{1/2}$$

$$= \frac{V_m}{2\sqrt{\pi}} \left[(\beta - \alpha) - \frac{1}{2} \{ \sin 2\beta - \sin 2\alpha \} \right]^{1/2}$$

Single-phase Full converter with R-L-E load. 435 M·H·R.

→ Here the load is assumed to be R-L-E. Voltage E may be due to a battery in the load ckt or may be generated emf of a dc motor.

→ The ckt arrangement of a 1-ϕ full converter is shown in the next page with a highly inductive load so that the load current is continuous and ripple free.

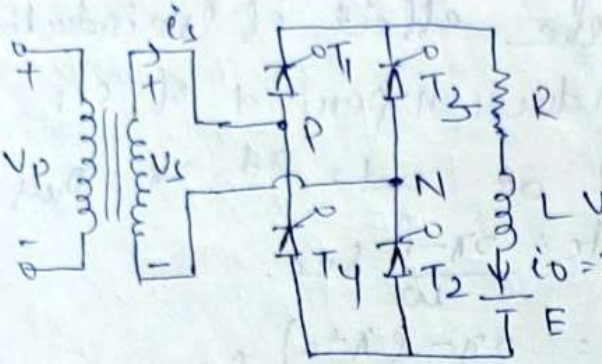


Fig- ckt diagram

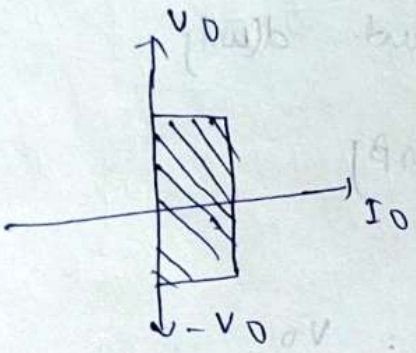


Fig- quadrant diagram

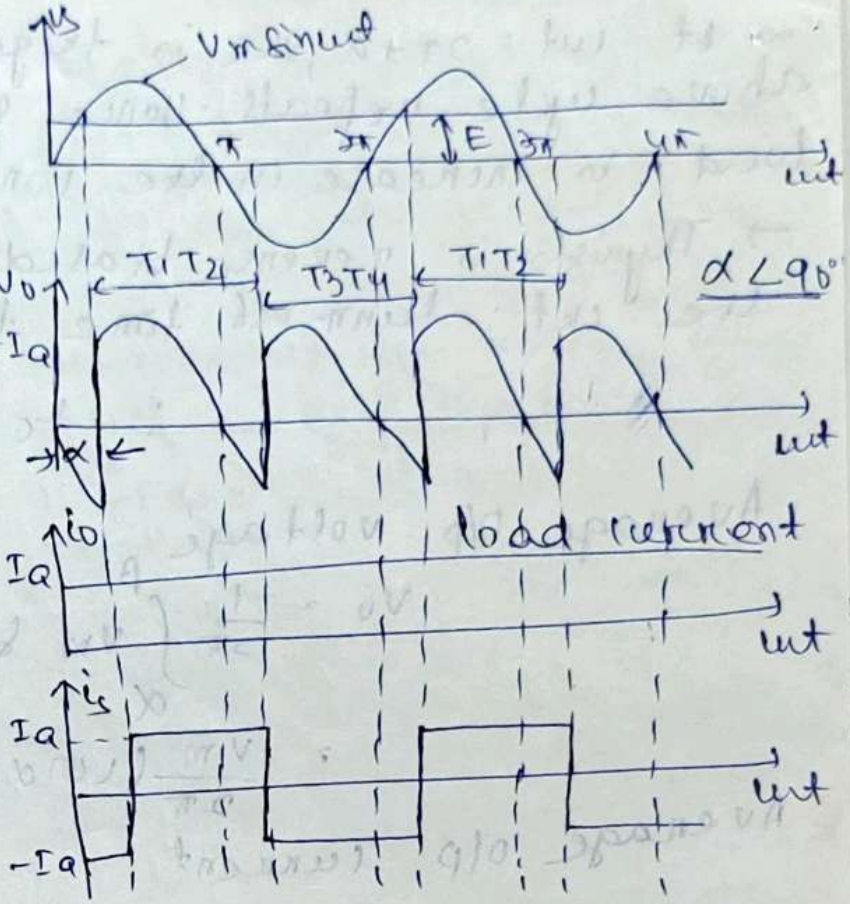


Fig - voltage and current waveforms for continuous load current.

→ During the +ve half-cycle, thyristors T_1 and T_2 are forward biased and when these two thyristors are fired simultaneously at $\omega t = \alpha$, load current path is P - T_1 - Load - T_2 - N. Due to inductive load thyristors T_1 and T_2 continue to conduct beyond $\omega t = \pi$, even though the input voltage is -ve.

→ During the -ve half-cycle of the input voltage, thyristors T_3 and T_4 are forward biased and firing of thyristors T_3 and T_4 applies the supply voltage across thyristors T_1 and T_2 as reverse blocking voltage.

T_1 and T_2 are turned off due to line or natural commutation and the load current is transferred from T_1 and T_2 to T_3 and T_4. Load current path is N - T_3 - load - T_4 - P.

→ During the period from α to π, i/p voltage v_s and input current is are positive and the power flows from supply to load. The converter is said to be operated in rectification mode.

→ During the period from π to $\pi+\alpha$, the i/p voltage v_s is -ve but the i/p current is is +ve and reverse power flows from the load to ac supply. The converter is said to be operated in inversion mode. The converter is extensively used in industrial applications up to 15 kW. In case of inversion mode, the net power flows from ac source to dc load because $(\pi-\alpha) > \alpha$.

→ Depending on the value of α, the average o/p voltage could be either +ve or -ve and it provides two-quadrant operation.

The average o/p voltage V_o is given by

$$V_{dc} = V_o = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi+\alpha} = \frac{2V_m}{\pi}\cos\alpha$$

The maximum average o/p voltage is $V_{dm} = \frac{2V_m}{\pi}$ and the normalized average o/p voltage is

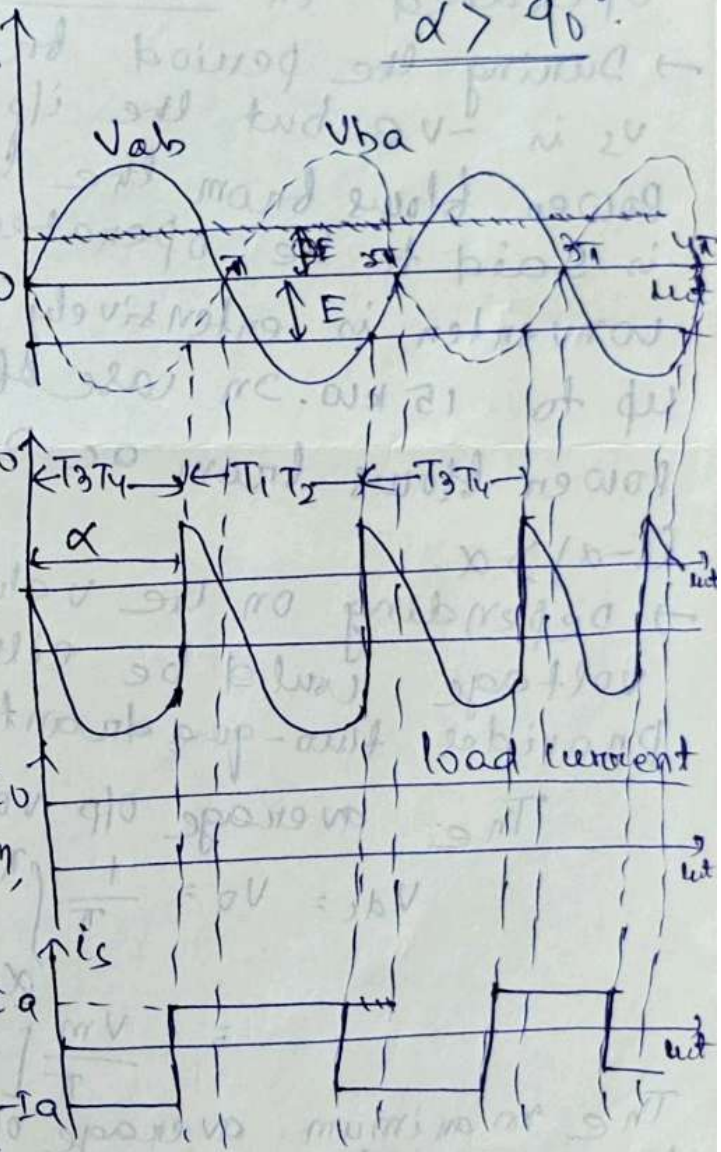
$$V_n = \frac{V_{dc}}{V_{dm}} = \cos\alpha$$

The rms value of o/p voltage is given by

$$V_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2} = \frac{V_m}{\sqrt{2}} = V_s$$

For $\alpha > 90°$, V_o is -ve. If the load ckt emf E is reversed, this source E will feed power back to ac supply. This operation of full converter is known as inverter operation of the converter. The full converter with firing angle delay greater than $90°$ is called line commutated inverter. Such an operation is used in the regenerative braking mode of a dc motor in which case, E is counter emf of the dc motor.

$\alpha > 90°$.



→ During 0 to α, ac source voltage v_s is +ve but is is -ve, power therefore flows from dc source to ac source. From α to π, both v_s & is are +ve, power therefore flows from ac source to dc source. But the net power flows from dc source to ac source because $(\pi - \alpha) < \alpha$.

→ In the converter operation, the average o/p voltage must be greater than load ckt emf E. During inverter operation, dc source voltage E must be more than inverter voltage V_o, only then power would flow from dc source to ac supply system. But in both converter & inverter mode, SCRs must be forward biased and current through SCRs must flow in same direction as SCRs are unidirectional devices.

Some key points. 440 M.H.R.

→ Varying the delay angle α from 0 to π, we can vary the average o/p voltage from $\frac{2V_m}{\pi}$ to $-\frac{2V_m}{\pi}$, Provided the load is highly inductive and it's current is continuous.

→ For a purely resistive load, the delay angle 'α' can be varied from 0 to $\pi/2$ producing an o/p voltage ranging from $\frac{2V_m}{\pi}$ to zero.

→ The full converter can operate in two quadrants for a highly inductive load and in one quadrant only for a purely resistive load.

3-φ converter.

Advantage of 3-φ converter over 1-φ converter.

1. In case of multiphase converter, load is always balanced and o/p power of the 3-φ converter is uniformly distributed in the three i/p lines. But in the case of 1-φ converter, it creates unbalance in the supply system.
2. As the number of pulses/cycles increases, duration of each pulse gets reduced. The o/p voltage will have lower fluctuations and it almost dc in nature. Hence harmonic content at the dc side is reduced with the increase in pulse number. So the quality of 3, 6, 12 pulse converter is better than single-pulse converter.
3. In case of 3-φ converters, the ripple frequency of the converter o/p voltage is higher than that of 1-φ converters. Thus the filtering requirement is less so a small size of inducton is required.

→ voltage regulation of 3-φ converter is better.

→ By increasing the pulse number, load current is continuous so the load performance is better.
→ The relative amount of ac ripple voltage at the o/p and the relative distortion factor decreases with the increase in pulse number.

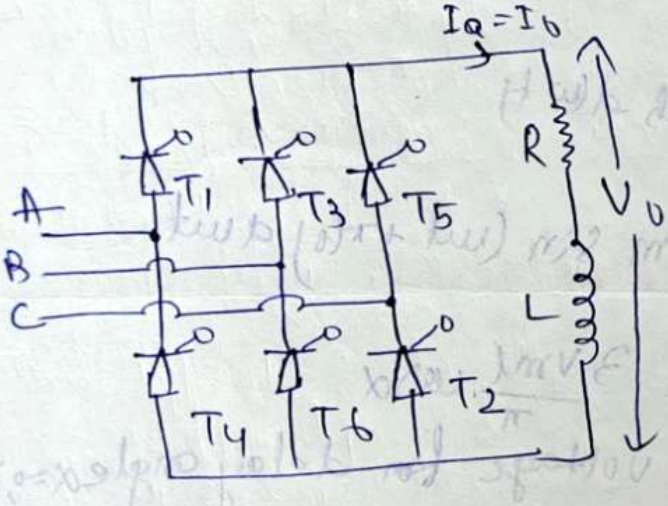
Classification of 3-ϕ converters.

1. 3-ϕ half-wave converters
2. 3-ϕ Semi converters
3. 3-ϕ Full converters
4. 3-ϕ Dual converters

→ 3-ϕ half-wave & Semi converter are 3-pulse converters. These are known as single-quadrant converters. Here each thyristor conducts for a period of 120°.
→ 3-ϕ full converters are 6-pulse converters. For every 60° firing angle each thyristor gets fired. This type of converters contain less ripples and the commutation process is easy in these ckts. Full converters are two quadrant converters.
→ 3-ϕ Dual converters is a twelve-pulse converter. Dual converters are four quadrant converters. when two six pulse converters are connected in antiparallel, a dual converter is formed.

3-ϕ Fully controlled converter with R-L load.

→ 3-ϕ converters are extensively used in industrial applications up to the 120kW level, where a two-quad quadrant operation is required. Figure below shows a 3-ϕ converter ckt with a highly inductive load. The thyristors are fired at an interval of π/3. The frequency of o/p ripple voltage is 6fs and the filtering requirement is less than that of half-wave converters.



T_1, T_3, T_5 are +ve group

T_2, T_4, T_6 are -ve group

→ During one cycle of o/p voltage, we are getting six pulses. So it is called 6-pulse 3-ϕ full-wave converter. Each cycle represent 360°.

If the line-to-neutral voltages (V_{ph}) are defined as

$V_a = V_m \sin \omega t$

$V_b = V_m \sin(\omega t - 120°)$

$V_c = V_m \sin(\omega t - 240°)$

$= V_m \sin(\omega t + 120°)$

Sequence.

A-C - 1-2

B-C - 2-3

B-A - 3-4

C-A - 4-5

C-B - 5-6

A-B - 6-1

The corresponding line to line voltages (V_L) are

$$V_{ab} = V_a - V_b = \sqrt{3}\, V_m \sin(\omega t + \pi/6)$$

$$V_{bc} = V_b - V_c = \sqrt{3}\, V_m \sin(\omega t - \pi/2)$$

$$V_{ca} = V_c - V_a = \sqrt{3}\, V_m \sin(\omega t + \pi/2)$$

Here T_1 is triggered at $\omega t = \pi/6$ i.e. 30°.

$T_3 = 150°$, $T_5 = 270°$

T_2 is triggered at 90°

$T_4 = 210°$, $T_6 = 330°$

The average o/p voltage is found from

$$V_o = V_{dc} = \frac{3}{\pi} \int_{\pi/6+\alpha}^{\pi/2+\alpha} v_{ab}\, d(\omega t)$$

$$= \frac{3}{\pi} \int_{\pi/6+\alpha}^{\pi/2+\alpha} \sqrt{3}\, V_m \sin(\omega t + \pi/6)\, d\omega t$$

$$= 3\sqrt{3}\frac{V_m}{\pi} \cos\alpha = \frac{3V_{ml}}{\pi}\cos\alpha$$

The maximum average o/p voltage for delay angle $\alpha = 0$, is

$$V_{dm} = \frac{3\sqrt{3}V_m}{\pi}$$

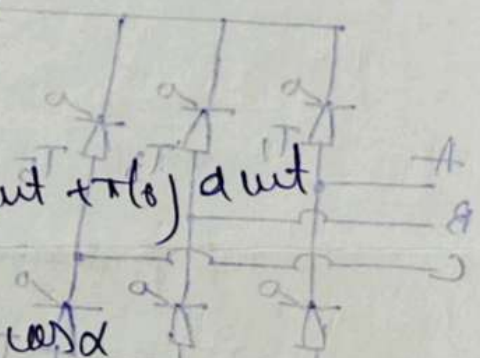
The normalized average o/p voltage is

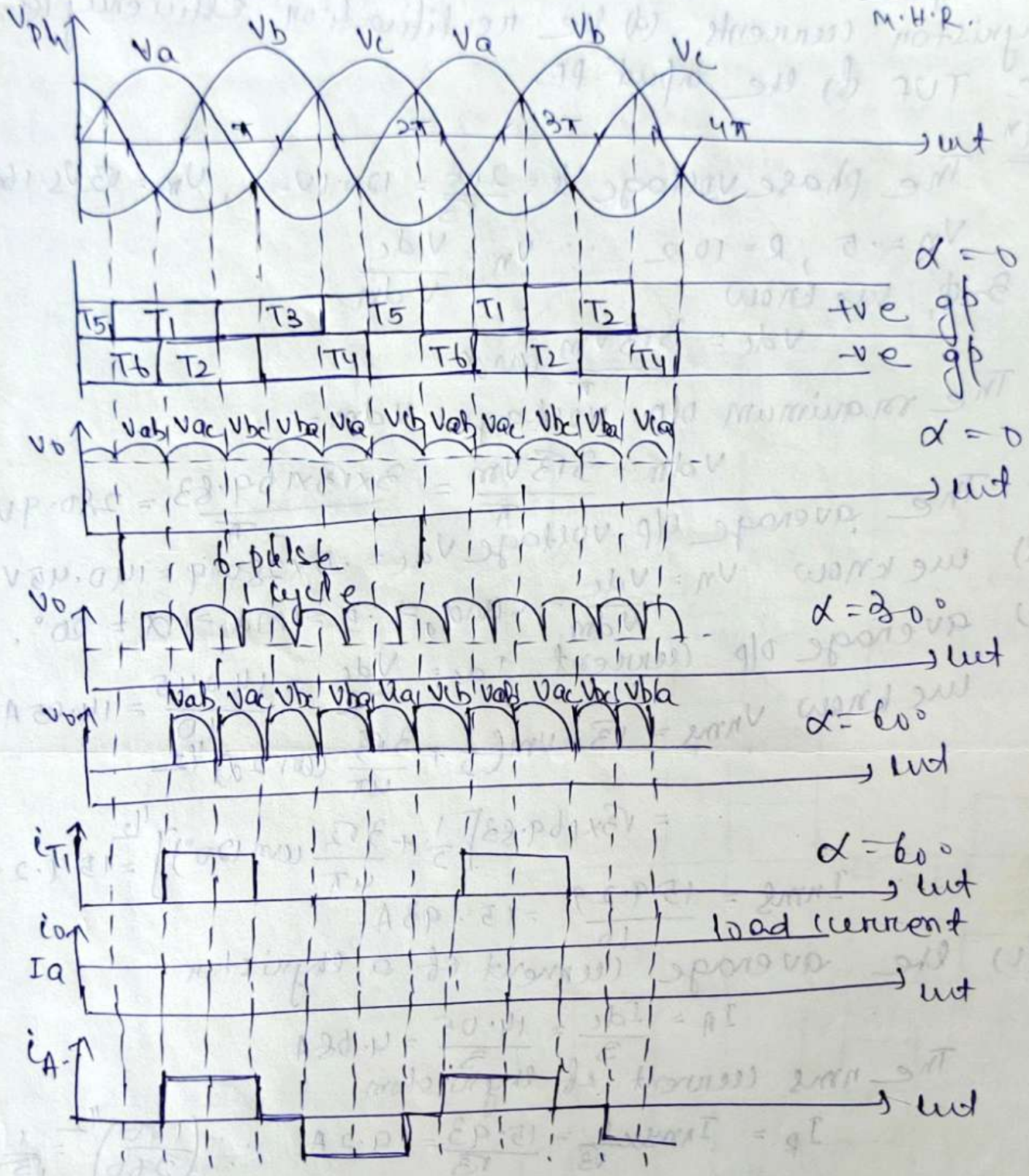
$$V_n = \frac{V_{dc}}{V_{dm}} = \cos\alpha$$

The rms value of o/p voltage is found from

$$V_{rms} = \left[\frac{3}{\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha} 3V_m^2 \sin^2(\omega t + \pi/6)\, d(\omega t)\right]^{1/2}$$

$$= \sqrt{3}\, V_m \left(\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}\cos 2\alpha\right)^{1/2}$$





Prob. A 3-ϕ Full-wave converter is operated from a 3-ϕ star-connected 208V, 60Hz supply and the load resistance R = 10Ω. If it is required to obtain an average o/p voltage of 50% of the maximum possible o/p voltage, calculate (a) the delay angle(α) (b) the rms and

1-φ Semiconverter.

467
M·H·R.

The ckt arrangement of a 1-φ semiconverter is shown below with a highly inductive load. The load current is assumed continuous and ripple free.

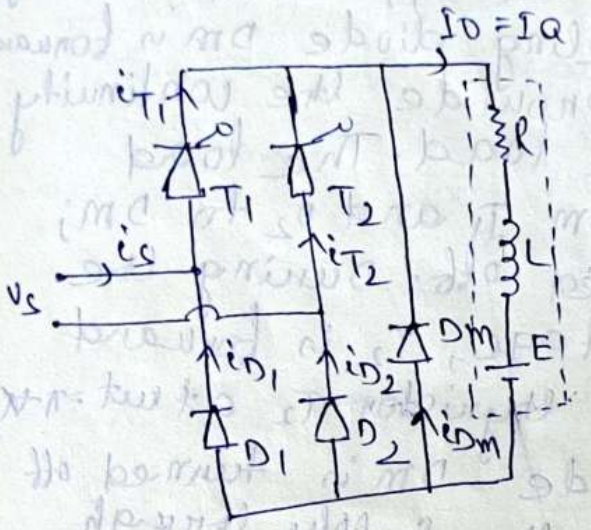
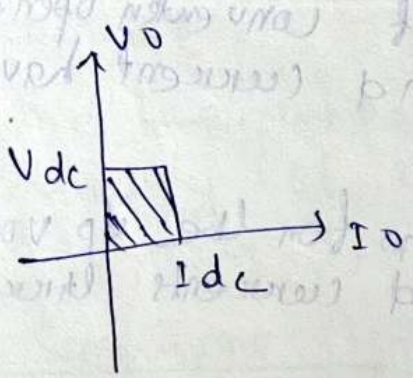


Fig. (a)



1st-quadrant operation

Fig. (b)

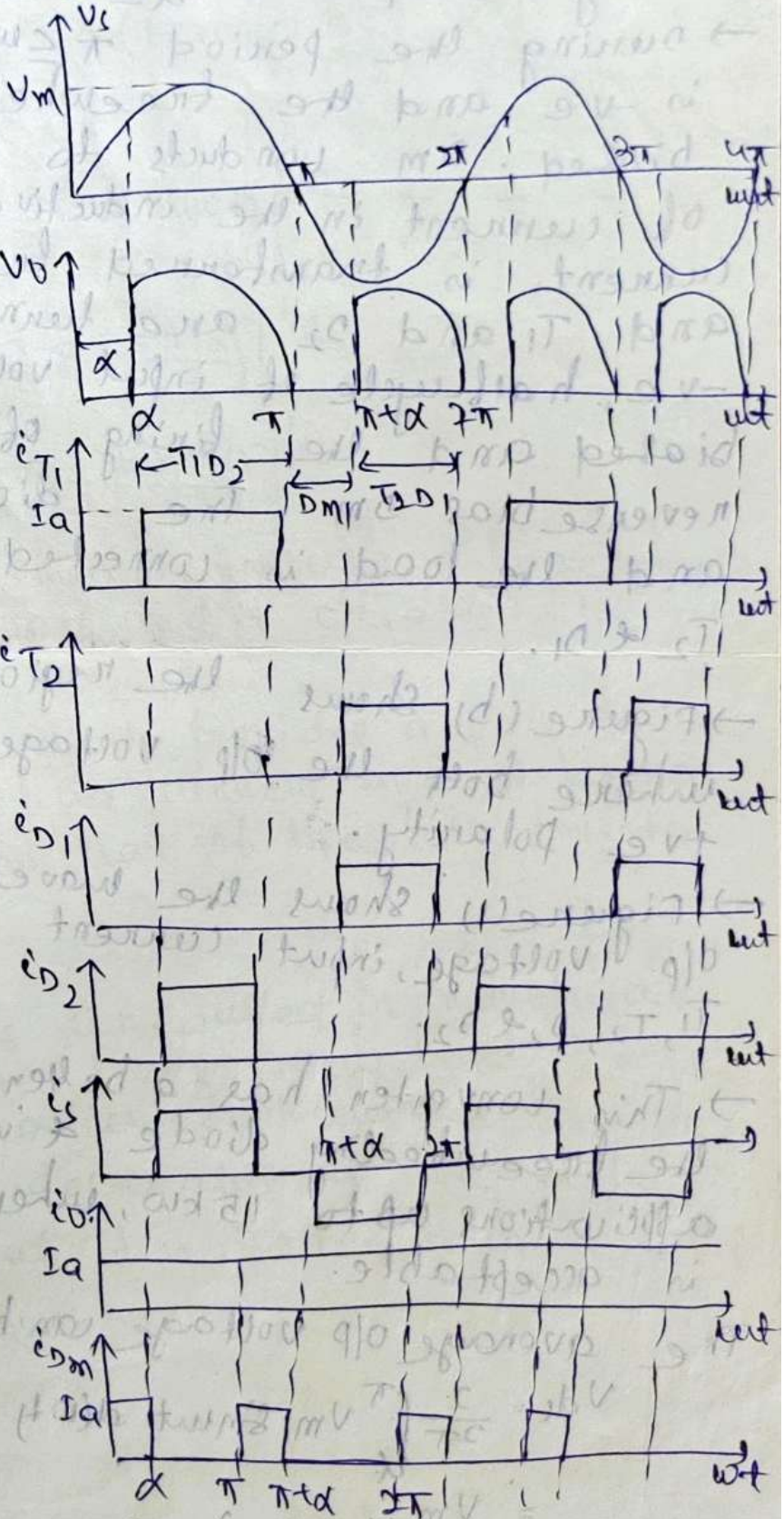


fig. -(c)

→ During the +ve half-cycle, SCR T_1 is forward biased. When T_1 is fired at $\omega t = \alpha$, the load is connected to the i/p supply through T_1 and D_2 during the period $\alpha \leq \omega t \leq \pi$.

→ During the period $\pi \leq \omega t \leq (\pi + \alpha)$, the input voltage is -ve and the freewheeling diode Dm is forward biased. Dm conducts to provide the continuity of current in the inductive load. The load current is transferred from T_1 and D_2 to Dm; and T_1 and D_2 are turned off. During the -ve half-cycle of input voltage, T_2 is forward biased and the firing of thyristor T_2 at $\omega t = \pi + \alpha$, reverse bias Dm. The diode Dm is turned off and the load is connected to the supply through T_2 & D_1.

→ Figure (b) shows the region of converter operation where both the o/p voltage and current have +ve polarity.

→ Figure (c) shows the waveforms for the i/p voltage, o/p voltage, input current and currents through T_1, T_2, D_2 & D_2.

→ This converter has a better power factor (PF) due to the freewheeling diode & is commonly used in applications upto 15 kW, where one-quadrant operation is acceptable.

The average o/p voltage can be found from

$$V_{dc} = \frac{2}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d(\omega t) = \frac{2V_m}{2\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi}$$

$$= \frac{V_m}{\pi}(1 + \cos\alpha)$$

The V_{dc} can be varied from $\frac{2V_m}{\pi}$ to 0 by varying α from 0 to π. The maximum average o/p voltage is $V_{dm} = \frac{2V_m}{\pi}$ and the normalized average o/p voltage is

$$V_n = \frac{V_{dc}}{V_{dm}} = .5(1+\cos\alpha)$$

The rms o/p voltage is

$$V_{rms} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\left(\pi-\alpha+\frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

$$= V_s\left[\frac{1}{\pi}\left(\pi-\alpha+\frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

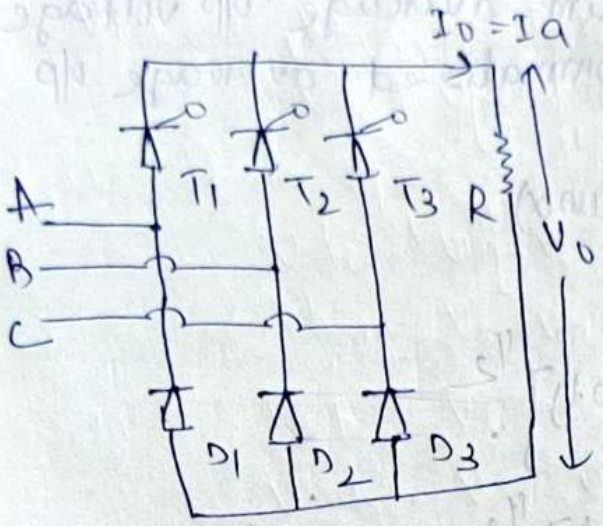
→ A single-phase semiconverter uses a freewheeling diode across the load and it operates in the 1st quadrant.

→ The freewheeling diode provides a path for the continuity of the load current and it has a better input PF than that of the full converter.

3-ϕ Semiconverter.

3-ϕ semiconverters are used in industrial applications up to the level 120kW level, where one-quadrant operation is required. The PF of this converter decreases as the delay angle increase, but it is better than that of 3-ϕ half-wave converters.

3-ϕ Semiconverter.



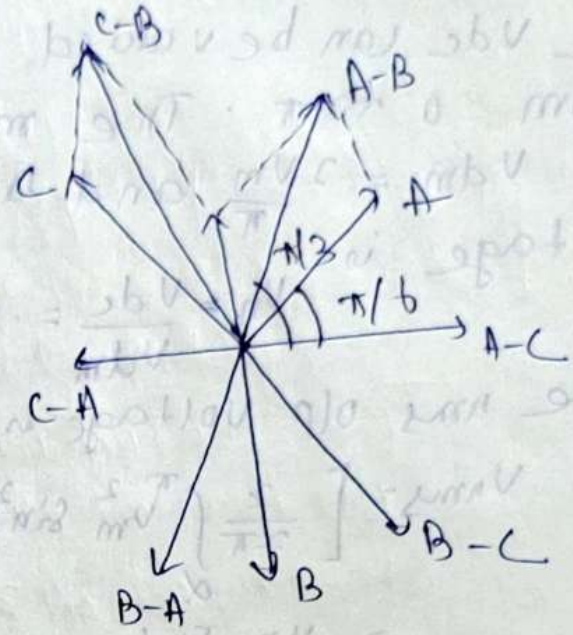
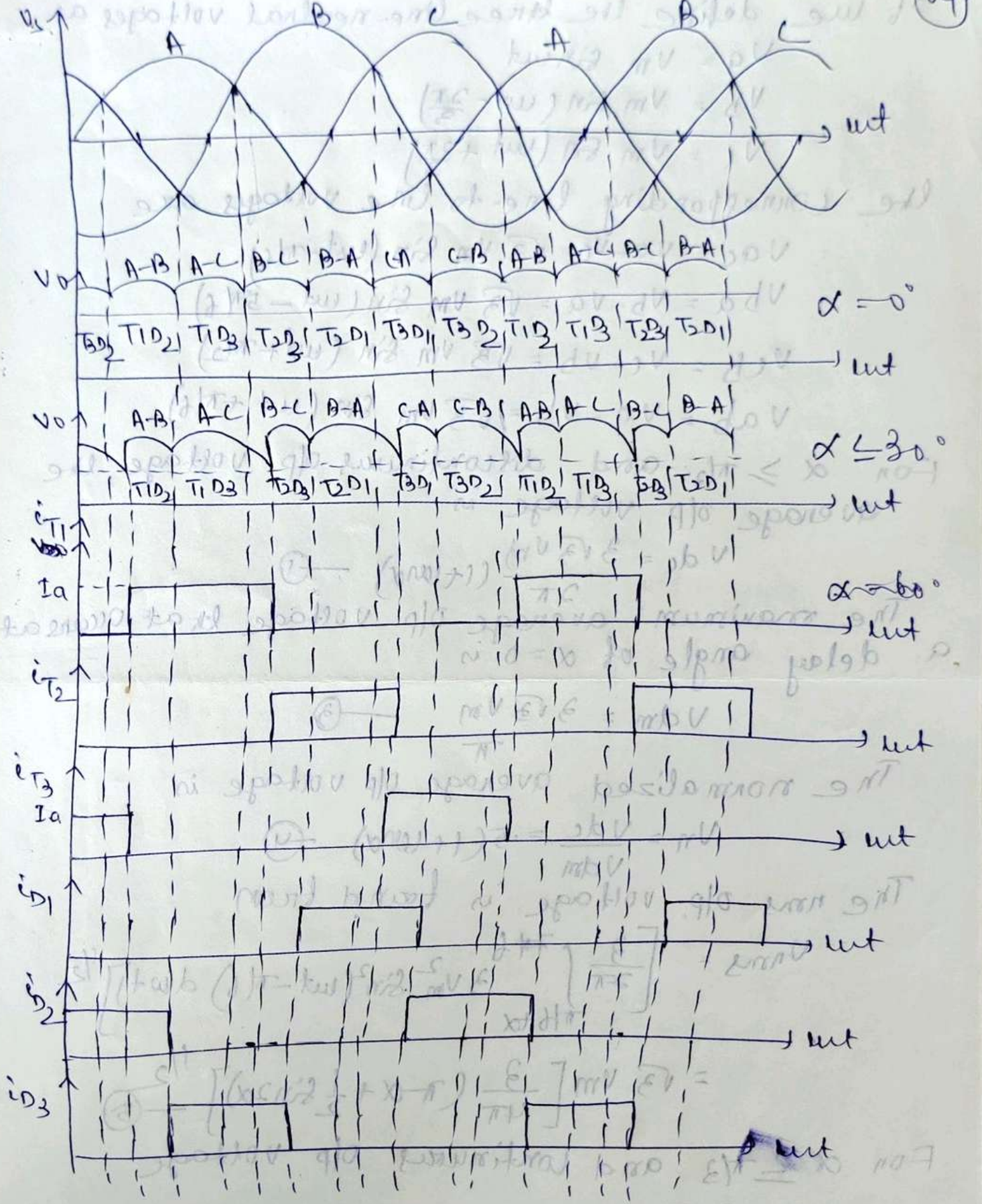


Fig- vector diagram for line voltage & phase voltage

Modes of operation for 0° firing angle	conducting phases	conducting devices
30-90° ⟶	A (phase) A-B line ⟶	$T_1 D_2$
90-150° ⟶	A (phase) A-C line ⟶	$T_1 D_3$
150°-210° ⟶	B (phase) B-C line ⟶	$T_2 D_3$
210°-270° ⟶	B (phase) B-A line ⟶	$T_2 D_1$
270-330° ⟶	C (phase) C-A line ⟶	$T_3 D_1$
330°-390° ⟶	C (phase) C-B line ⟶	$T_3 D_2$


A
B
C
A
B
C
ωt
A-B A-C B-C B-A C-A C-B A-B A-C B-C B-A
V_o
T_3D_2 T_1D_2 T_1D_3 T_2D_3 T_2D_1 T_3D_1 T_3D_2 T_1D_2 T_1T_3 T_2D_3 T_2D_1
$\alpha = 0°$
ωt
V_o
A-B A-C B-C B-A C-A C-B A-B A-C B-C B-A
T_1D_2 T_1D_3 T_2D_3 T_2D_1 T_3D_1 T_3D_2 T_1D_2 T_1D_3 T_2D_3 T_2D_1
$\alpha \leq 30°$
ωt
i_{T_1}
I_a
$\alpha = 60°$
ωt
i_{T_2}
ωt
i_{T_3}
I_a
ωt
i_{D_1}
ωt
i_{D_2}
ωt
i_{D_3}
ωt

Diode of T_1 and T_2 are kept left open. Th...

Ac voltage controllers [Ac to Ac]

Ac voltage controller is a device which converts fixed Ac voltage to variable Ac voltage at the same frequency by using line commutation.

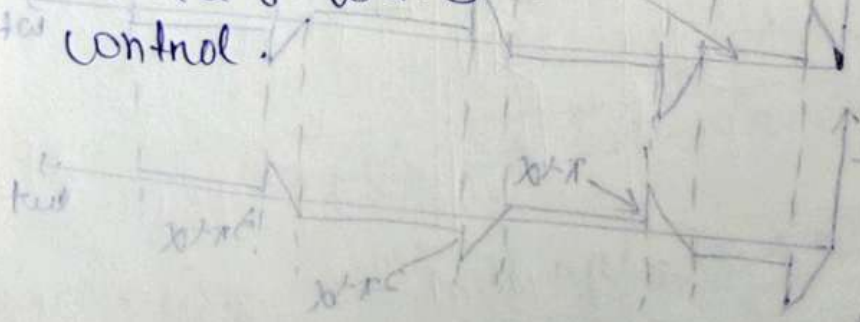
→ some of the applications of ac voltage controllers are for domestic and industrial heating, transformer tap changing, lighting control, speed control of 1-ϕ and 3-ϕ ac drive and ac magnet controls.

→ For power transfer, two types of control are normally used.

1. on-off control
2. phase-angle control.

In on-off control, thyristor switches connect the load to the ac source for a few cycles of input voltage and then disconnect it for another few cycles. In phase control, thyristor switches connect the load to the ac source for a portion of each cycle of input voltage.

→ The ac voltage controllers can be classified into two types; (1) 1-ϕ controllers and (2) 3-ϕ controllers with each type subdivided into (a) unidirectional or half-wave control (b) bidirectional or full-wave control.



1-φ bidirectional controllers with R-load.

→ Although the half-wave controller can vary the o/p voltage by varying the delay angle α, the o/p contains an undesirable dc component. The problem of dc current can be prevented by using bidirectional or (full-wave) control and a single-phase full-wave controller with a resistive load is shown below.

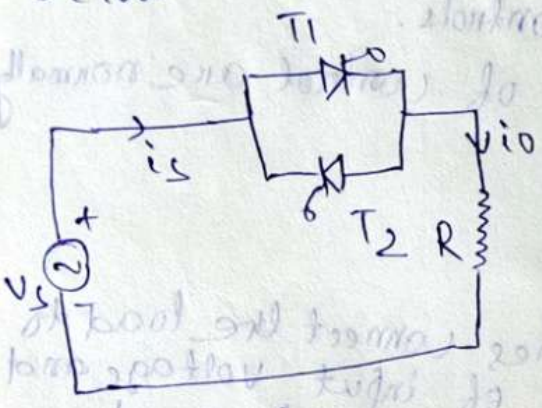


Fig.(a)

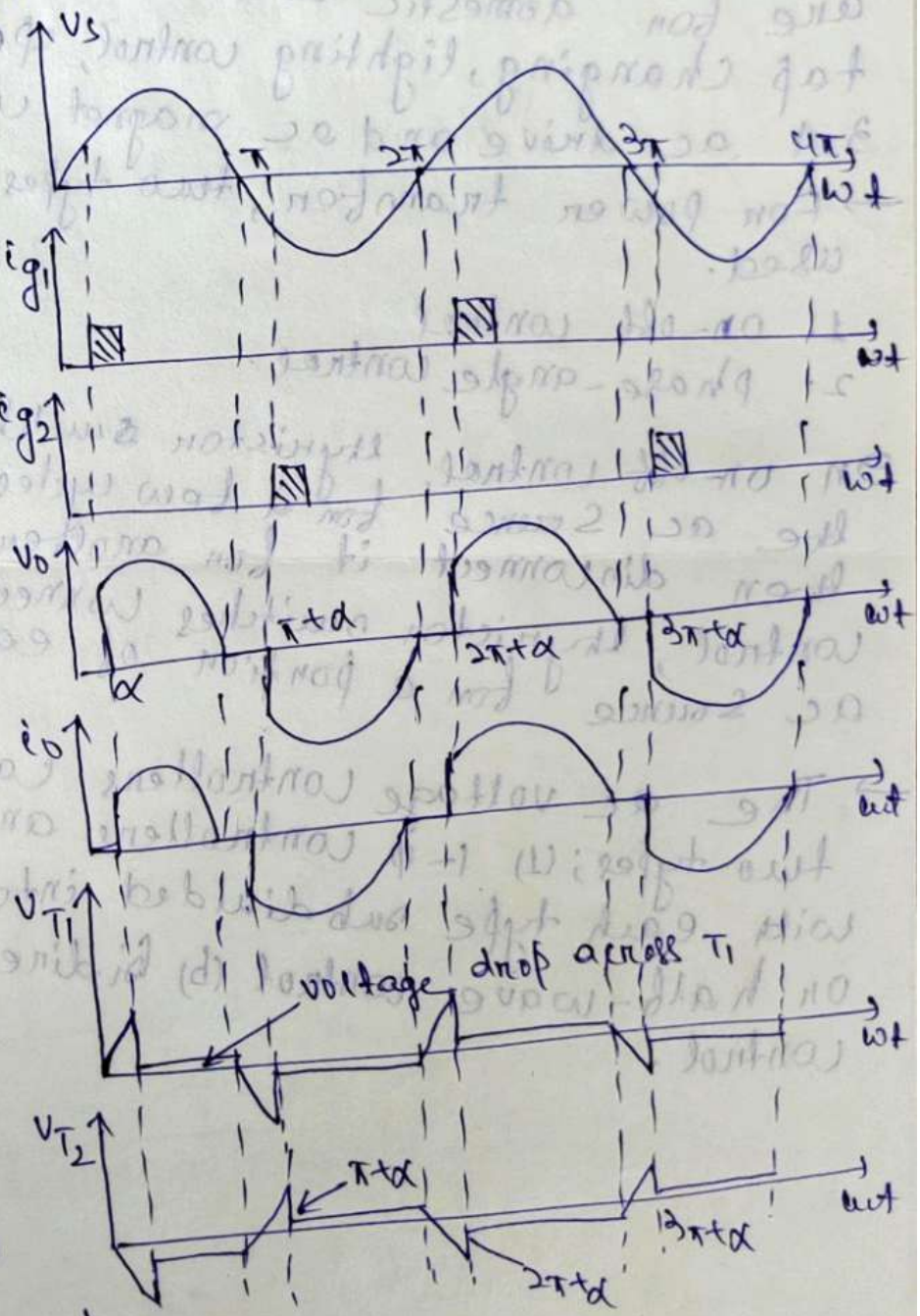


Fig-(b)

→ During the +ve half-cycle of input voltage, the power flow is controlled by varying the delay angle of T_1 and T_2 controls the power flow during the -ve half-cycle of input voltage. The firing

Pulses of T_1 and T_2 are kept 180° apart. The waveforms for the input voltage, O/P voltage, and gating signals of T_1 and T_2 are also shown in fig-(b).

If $v_s = \sqrt{2} V_s \sin \omega t$ is the input voltage, the rms O/p voltage can be found from

$$V_o = \left[\frac{1}{\pi} \int_{\alpha}^{\pi} 2 V_s^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$= \left[\frac{V_s^2}{\pi} \int_{\alpha}^{\pi} (1 - \cos 2\omega t) \, d(\omega t) \right]^{1/2}$$

$$= V_s \left[\frac{1}{\pi} \left(\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2}$$

→ By varying α from 0 to π, v_o can be varied from V_s to 0. where V_s is the rms value of source voltage.

→ In fig. (a), the gating ckts for T_1 and T_2 must be isolated. It is possible to have a common cathode for T_1 & T_2 by adding two diodes as shown below.

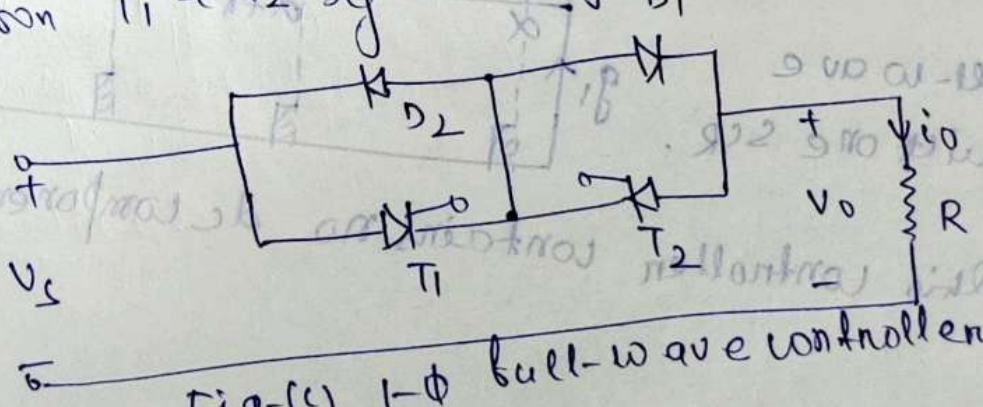


Fig-(c) 1-ϕ full-wave controller with common cathode.

→ During +ve half-cycle T_1 & D_1 conducts and Thyristor T_2 and diode D_2 conduct during the -ve half-cycle. Due to two power devices conducting at the same time, the conduction losses of devices would increase

and efficiency would be reduced.

→ A 1-ϕ full-wave controller can also be implemented with one thyristor and four diode as shown below. The four diodes act as bridge rectifier. The voltage across thyristor T_1 and it's current are always unidirectional. Three power devices conduct at the same time the efficiency is also reduced.

→ The bridge rectifier and thyristor or (transistor) act as a bidirectional switch. which is commercially available as a single device with a relatively low on-state conduction loss.

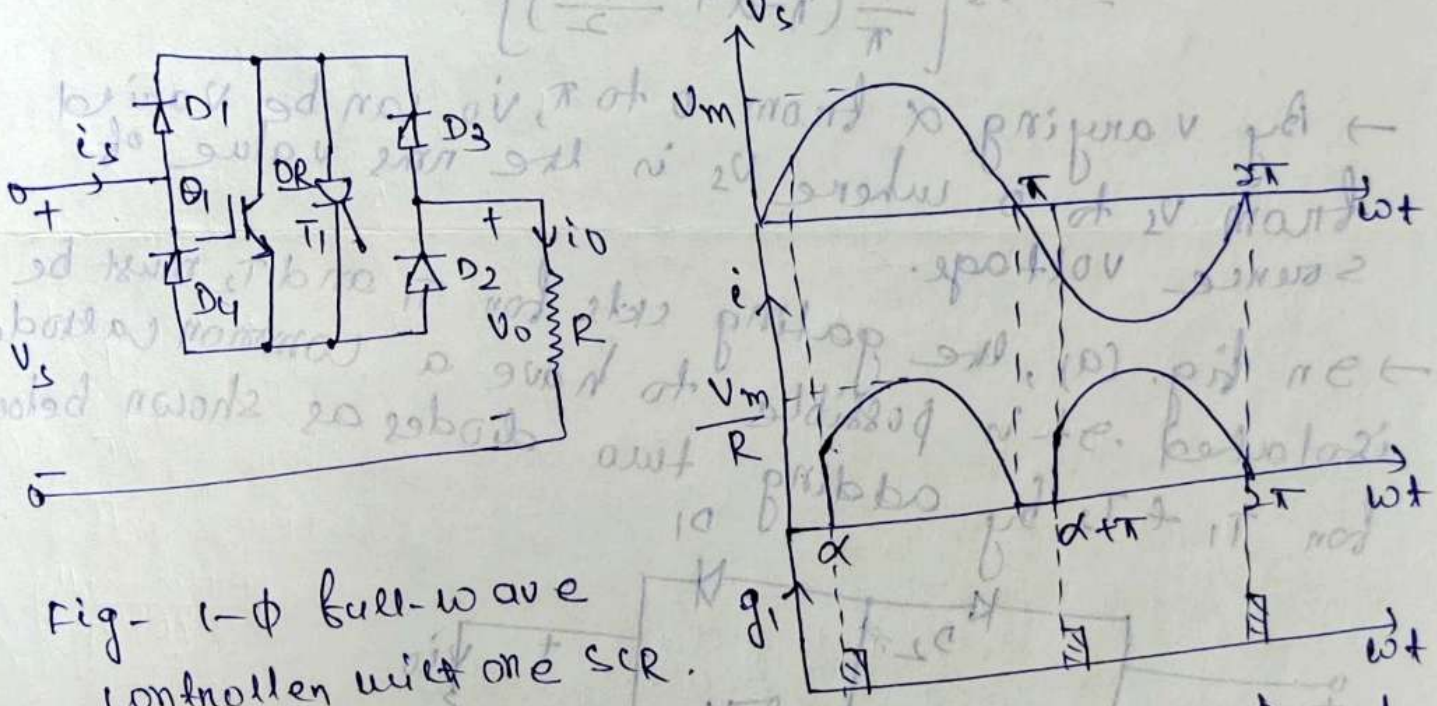


Fig- 1-ϕ full-wave controller with one SCR.

→ The dp of this controller contains no dc component.

~~Prob~~ A 1-ϕ

1-φ cyclo converter (step-down)

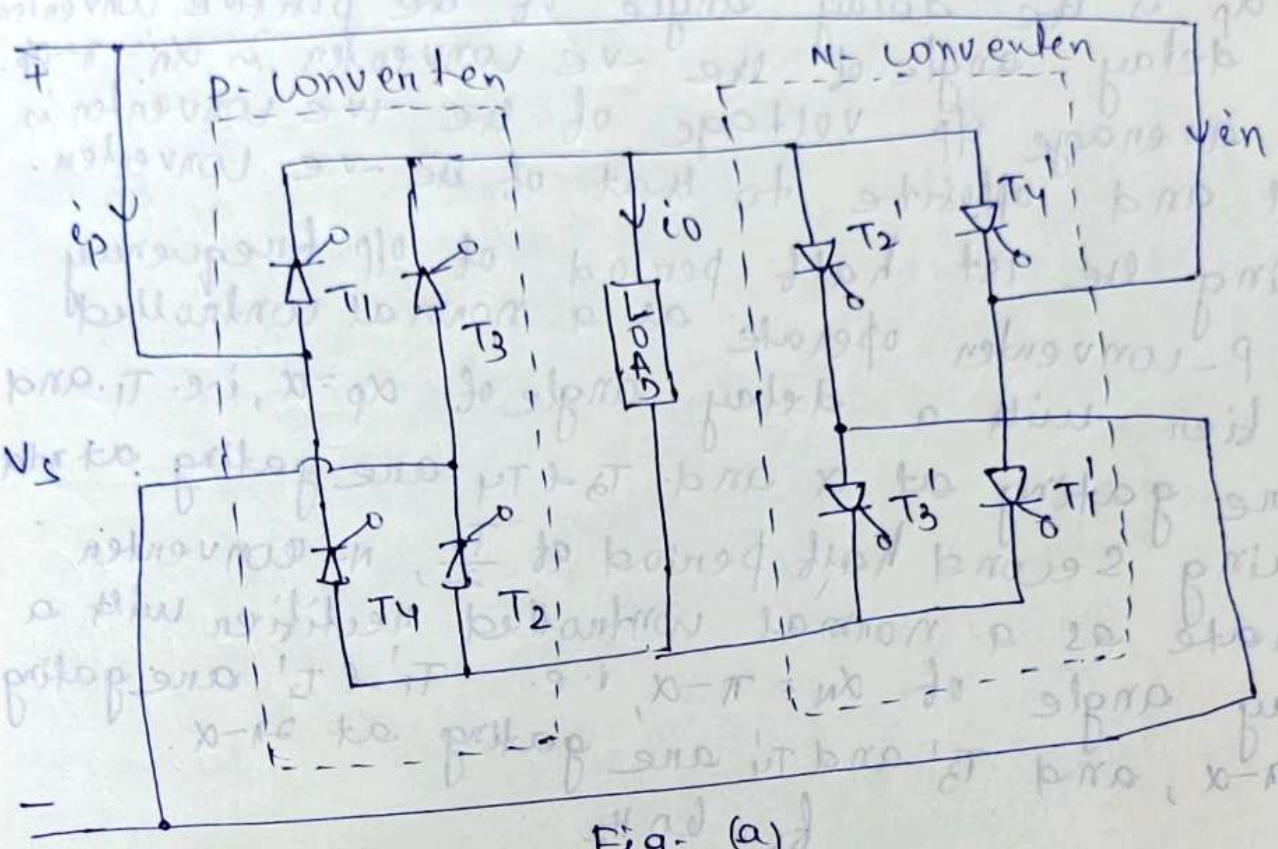


Fig. (a)

Here T_1, T_2, T_3, T_4 — +ve group converter

T_1', T_2', T_3', T_4' - -ve group converter

→ Here two 1-φ controlled converters are operated as bridge rectifier. Their delay angle are such that the o/p voltage of one converter is equal and opposite to that of other converter. i.e. $\boxed{V_{dc2} = -V_{dc1}}$

If converter P is operating alone, the average o/p voltage is +ve and if converter N is operating, the o/p voltage is -ve.

Fig. (b) shows the waveforms for the o/p voltage and gating signals for positive and negative converters with the +ve converter on for time $\frac{T_o}{2}$ and the -ve converter operating for time $\frac{T_o}{2}$.

The frequency of the o/p voltage is $f_o = \frac{1}{T_o}$.

→ If α_p is the delay angle of the positive converter, the delay angle of the -ve converter is $\alpha_n = \pi - \alpha_p$. The average o/p voltage of the +ve converter is equal and opposite to that of the -ve converter.

→ During the 1st half period of o/p frequency $\frac{T_o}{2}$, P-converter operate as a normal controlled rectifier with a delay angle of $\alpha_p = \alpha$, i.e. T_1 and T_2 are gating at α and T_3 & T_4 are gating at $\pi+\alpha$.

→ During second half period of $\frac{T_o}{2}$, N-converter operate as a normal controlled rectifier with a delay angle of $\alpha_N = \pi - \alpha$, i.e. T_1' & T_2' are gating at $\pi-\alpha$, and T_3' and T_4' are gating at $2\pi-\alpha$.

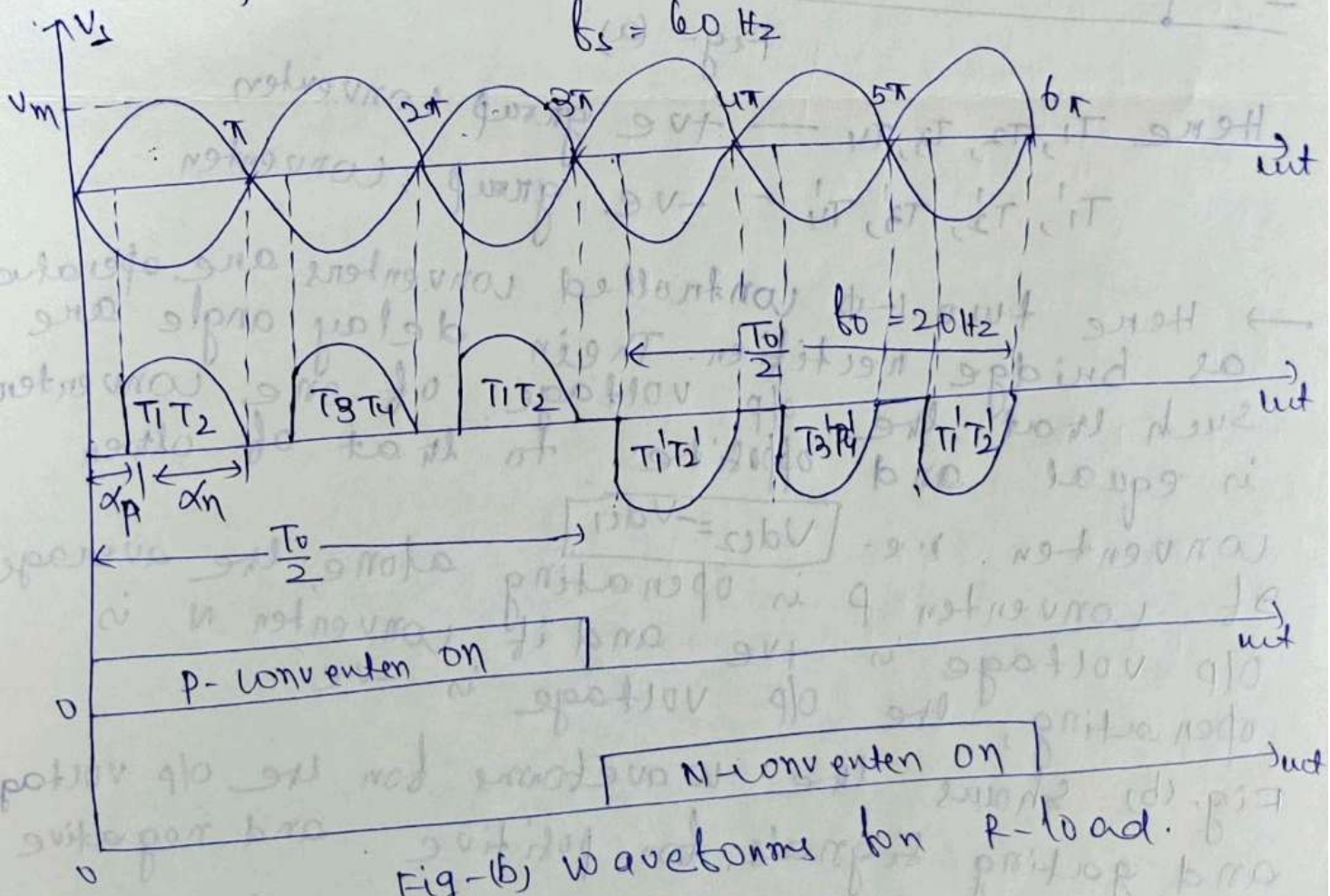


Fig-(b) Waveforms for R-load.

Here $f_o = 20$ Hz.

Cyclo-converter

→ A circuit which converts i/p power at one frequency to o/p power at a different frequency with one-stage conversion is called a cycloconverter. A cycloconverters is thus a one-stage Frequency changer.

→ Basically cycloconverters are 2 types

(i) Step-down cycloconverters ~~and~~ $(f_o < f_s)$

(ii) Step-up cycloconverter. $(f_o > f_s)$

✱ Applications of cycloconverters:-

→ Speed control of High-power Ac drives

→ Induction Heating

→ Static VAr compensation

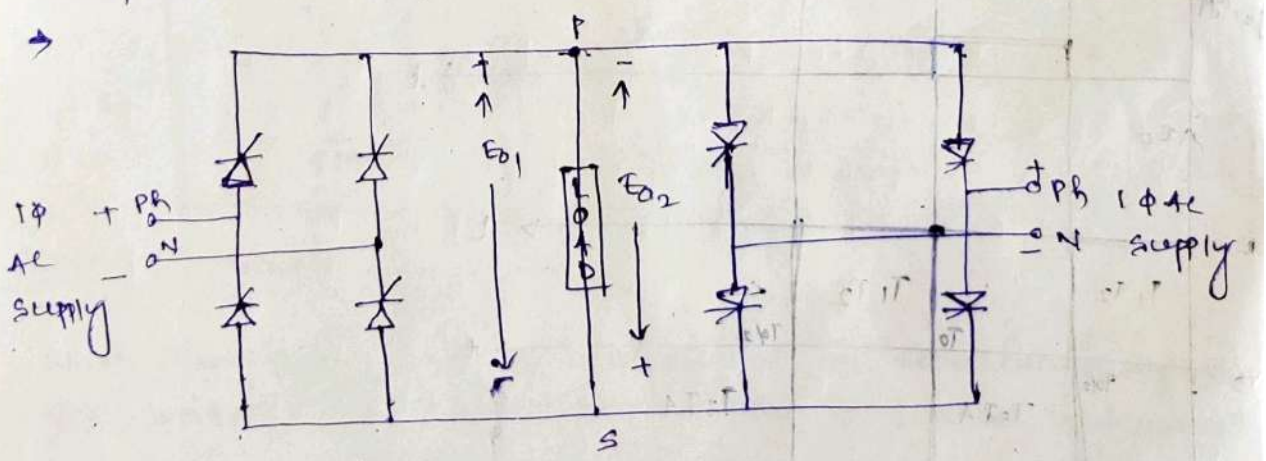
→ For converting variable-speed alternator voltage to constant frequency o/p. Vtg for use as power supply in aircraft or shipboards.

✱ Bridge Type step up cycloconverters:-

→ The SCRs are arranged in a bridge type and hence, it is known as bridge type cycloconverter consisting of 8 SCRs.

P_1, P_2, P_3, P_4 thyristors constitute positive group where as N_1, N_2, N_3, N_4 thyristors constitute negative group. Load is connected b/w the two Bridges which are connected in "antiparallel.

→



Operation principle :-

Mode-1 $(0 < \omega t < \pi)$

→ During the positive half cycle of the supply voltage P_1, P_2, N_3, N_4 are forward biased. From $\omega t = 0$ to π. Initially P_1 & P_2 thyristor triggered. The load voltage now follows the positive envelope of the supply voltage. The circuit completes its path through.

$$Ph - P_1 - P - Load - S - P_2 - N$$

→ At the instant ωt_1, P_1 & P_2 are turned off due to Forced commutation. Now, N_3 & N_4 triggered which already in Forward biased condition during +ve half cycle. The load o/p v-tg traces the negative envelope of the supply voltage. The direction of current $Ph - N_3 - S - Load - P - N_4 - N$

→ At ωt_2, N_3 & N_4 are forced commutated and P_1 and P_2 are turned ON. The load voltage is Now positive and follows the positive envelope. This process continues for positive half cycle of source voltage till $\omega t = \pi$ rad.

Mode-2 $\pi < \omega t < 2\pi$

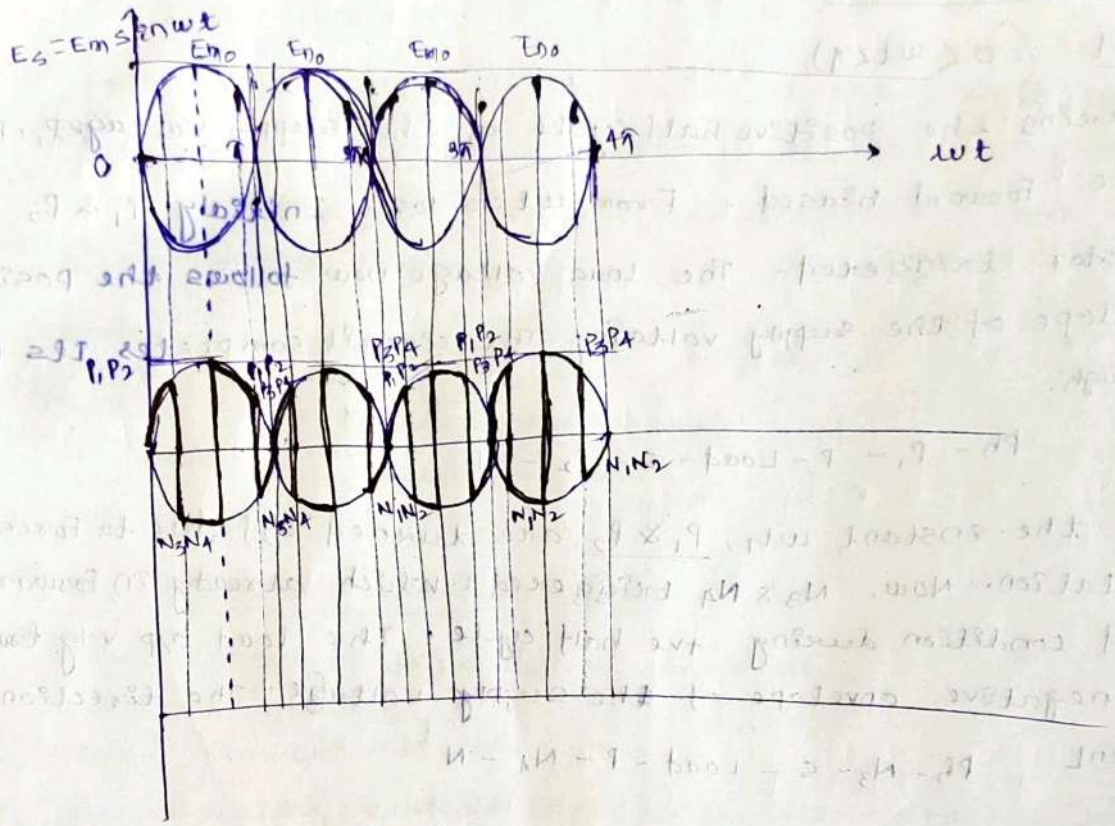
→ During the negative half cycle of the source voltage, thyristors P_3, P_4, N_1, N_2 are forward Biased. Give the gate signal to P_3 & P_4 thyristors Where the load voltage Follows the +ve envelope of the supply voltage. The circuit completes Path

$$N - P_3 - P - Load - S - P_4 - Ph$$

→ At the instant ωt_4, P_3 and P_4 are Forced commutated. Give the gate signal to thyristors N_1 & N_2 Which are already in forward biased condition. Now the o/p traces the negative envelope of the supply voltage. The circuit completes its path as

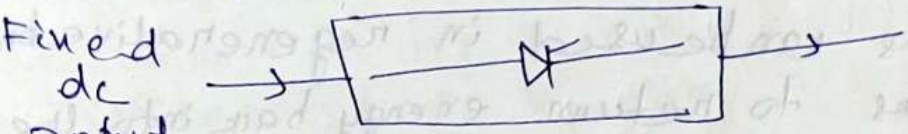
$$N - N_1 - S - Load - P - N_2 - Ph$$

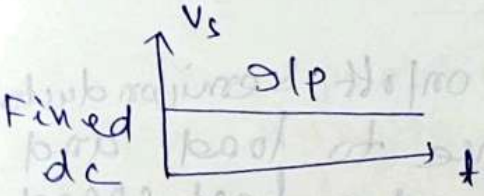
→ At $\omega t = \omega t_5$, N_1 & N_2 are forced commutated. Its associated Waveforms.

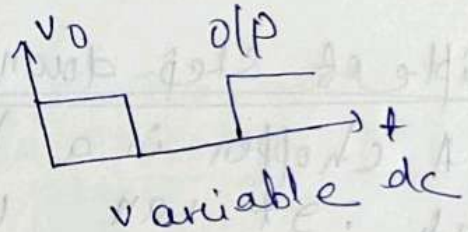

$E_s = E_m \sin \omega t$
E_{mo}
E_{mo}
E_{mo}
E_{mo}
0
π
2π
3π
4π
ωt
$P_1 P_2$
$P_3 P_4$
$P_3 P_4$
$P_1 P_2$
$P_3 P_4$
$P_3 P_4$
$N_1 N_2$
$N_2 N_1$
$N_3 N_4$
$N_1 N_2$
$N_1 N_2$

DC choppers

A chopper is a static device that converts fixed dc i/p voltage to variable dc d/p voltage directly.







A dc converter (chopper) may be considered as dc equivalent of an ac transformer with a continuously variable turn ratio. Like a transformer it can be used to step-down or step-up a dc voltage source.

AC link chopper. → In an ac link chopper, dc is 1st converted to ac by an inverter. Ac is then stepped-up or stepped down by a transformer which is then converted to dc by a rectifier. Ac link chopper is a two stage converter i.e. dc to Ac and then ac to dc. Ac link chopper is costly and less efficient as compared to dc chopper.

Application They are used for traction motor control in electric automobiles, trolley cars, mine haulers, marine hoists (lift, elevators)

Advantage of chopper.

1. It provides smooth speed control.
2. losses are low, high efficiency
3. Fast dynamic response
4. DC converters can be used in regenerative braking of dc motors to return energy back into the supply

Principle of step-down chopper.

A chopper is a high speed on/off semiconductor switch. It can connect source to load and disconnect the load from source at a fast speed.

Here the chopper is represent by a switch 'SW' inside a dotted rectangle which may be turned on or turned off as desired.

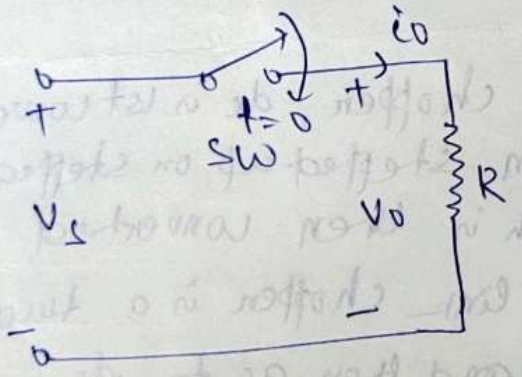


Fig. (a)

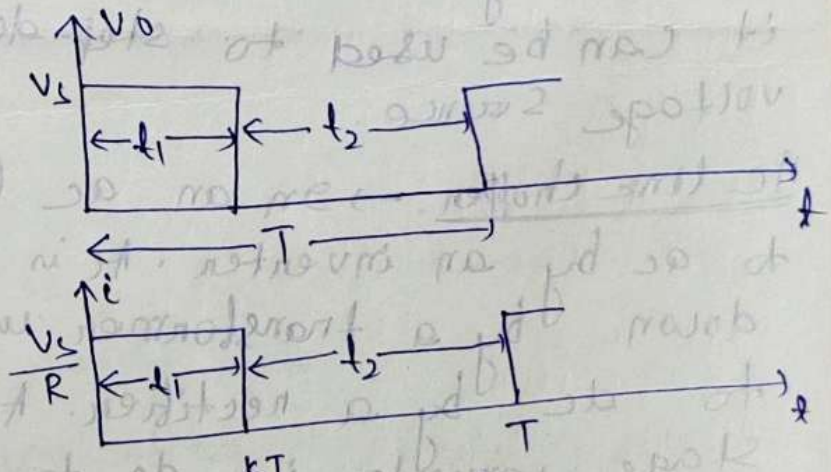


Fig-(b)

$t = 0^+$ the instant just after the switching operation

$t = 0^-$ the instant just before the switching operation.

→

when switch 'sw' known as the chopper is closed for a time t_1, the input voltage v_s appear across the load. If the switch remains off for a time t_2, the voltage across the load is zero. The waveforms for the o/p voltage and load current are shown in fig. (b). The converter switch can be implemented by using a 1. BJT. 2. MOSFET 3. GTO or 4. IGBT.

→ The practical devices have a finite voltage drop ranging from .5 to 2 v. and for simplicity we neglect the voltage drops of these power semiconductor devices.

Here $t_1 = t_{on}$ = on-time

$t_2 = t_{off}$ = off-time

The average load voltage v_o is given by

$$v_o = \frac{T_{on}}{T_{on}+T_{off}} v_s = \frac{T_{on}}{T} v_s = \alpha v_s \quad \text{---(1)}$$

where $T = T_{on} + T_{off}$ = chopping period

$\alpha = \frac{T_{on}}{T}$ = duty cycle.

Thus v_o can be controlled by varying duty cycle α. Eqn (1) shows that v_o is independent of load current.

eqn (1) can be written as

$$\boxed{v_o = f \cdot T_{on} \cdot v_s}$$

where $f = \frac{1}{T}$ = chopping frequency.

The average o/p voltage can also be found by

$$V_a = \frac{1}{T}\int_0^{t_1} v_o \, dt = \frac{t_1}{T} V_s = f t_1 V_s = k V_s.$$

$$\boxed{V_a = k V_s}$$

where k = is duty cycle.

The average load current is given by

$$I_a = \frac{V_a}{R} = \frac{k V_s}{R}.$$

where $k = \frac{t_1}{T}$ is the duty cycle of chopper.

f = is the chopping frequency.

The rms value of o/p voltage is found from

$$V_{or} = \left[\frac{1}{T}\int_0^{kT} v_o^2 \, dt\right]^{1/2} = \sqrt{k} \cdot V_s. \quad \text{---(2)}$$

Assuming a lossless converter, the input power to the converter is the same as the o/p power and is given by

$$P_i = \frac{1}{T}\int_0^{kT} v_o \cdot i \, dt = \frac{1}{T}\int_0^{kT} \frac{v_o^2}{R} dt = k\frac{V_s^2}{R}$$

The effective i/p resistance seen by the source is

$$R_i = \frac{V_s}{I_a} = \frac{V_s}{\frac{kV_s}{R}} = \frac{R}{k}.$$, which indicates that the converter makes the i/p resistance R_i as a variable resistance of R/k.

→ ~~The variation~~

The variation of the normalized i/p resistance against the duty cycle is shown below.

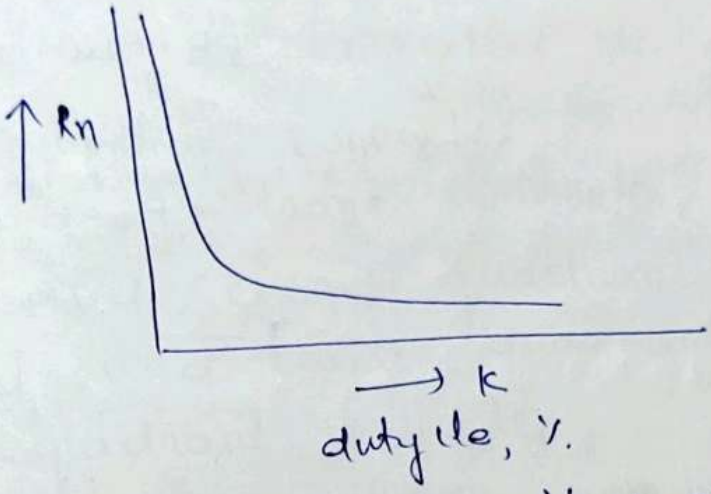


Fig. Effective i/p resistance against K.

→ The duty cycle k can be varied from 0 to 1 by varying t_1, T on t. Therefore the o/p voltage V_o can be varied from 0 to V_s by controlling k, and the power flow can be controlled.

1. Constant-frequency operation. The converter on switching, frequency f (or chopping period) is kept constant and on-time t_1 is varied. variation of Ton or t_1 means adjustment of pulse width. This type of control is known as pulse-width-modulation (PWM) control. This is also known as TRC. (time ratio control)

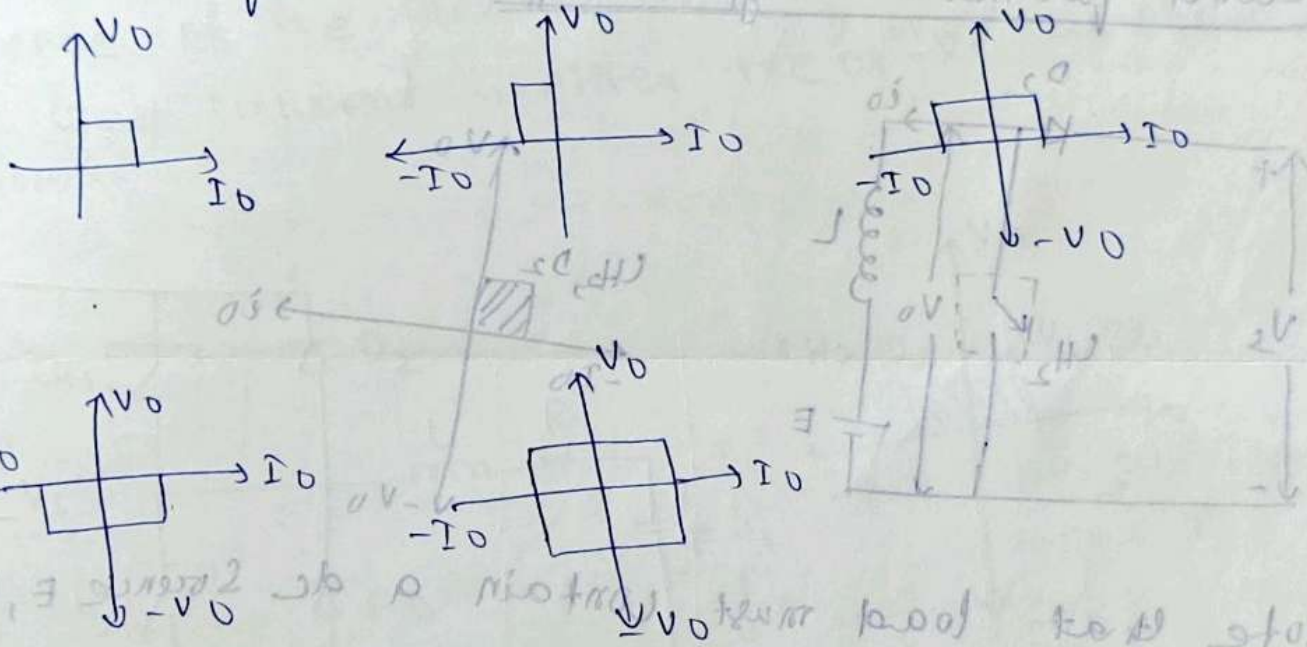
2. Variable-frequency operation.

In this operation chopping frequency f is varied and either on-time t_1 or off-time t_2 is kept constant. This is called frequency modulation. This type of control would generate harmonics at unpredictable frequencies and the filter design would be difficult.

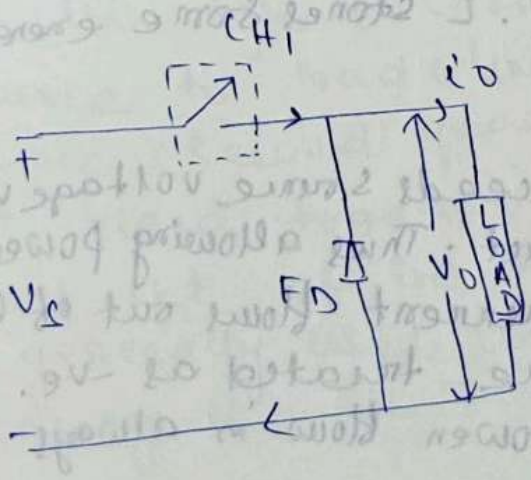
Converter classification. 182 M·H·R.

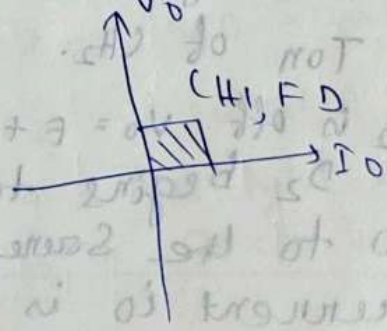
Depending on the direction of current and voltage flow, dc converters can be classified into

1. First quadrant converter.
2. Second quadrant converter
3. First and second quadrant converter.
4. Third and fourth quadrant converter.
5. Four-quadrant converter.



1st quadrant or type-A chopper.

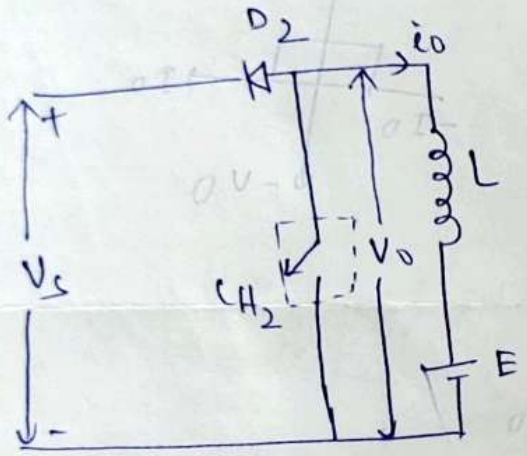


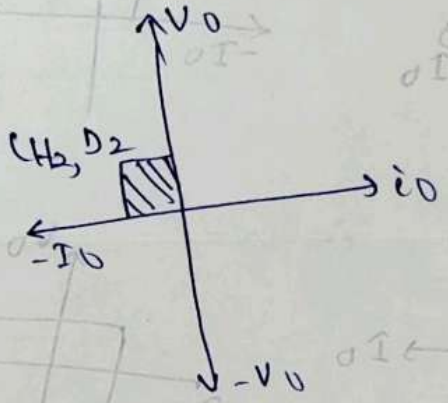


When chopper CH_1 is ON, $V_0 = V_s$ and current i_0 flows in the arrow direction. When CH_1 is off $V_0 = 0$ but i_0 is flowing in FD. It is thus seen that average values of both load voltage & current i.e. V_0 & i_0 are always +ve.

The power flow in type-A chopper is always from source to load. This chopper is also called step-down chopper as average o/p voltage V_0 is always less than the input dc voltage V_s.

Second-quadrant or type B chopper.





Note that load must contain a dc source E, like a battery in this chopper.

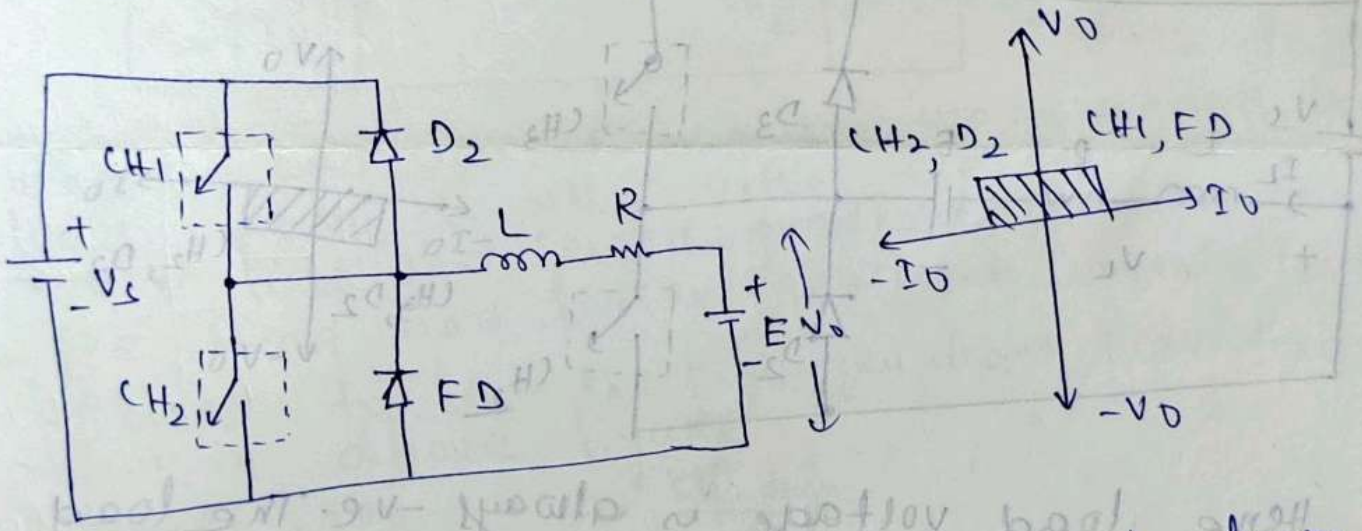
When CH_2 is on, $V_0 = 0$ but load voltage E drives current through L and CH_2. L stores some energy during Ton of CH_2.

When CH_2 is off $V_0 = E + L\frac{di}{dt}$ exceeds source voltage V_s. As a result D_2 begins to conduct. Thus allowing power to flow to the source. i.e. current flows out of the load, current i_0 is therefore treated as -ve. Since V_0 is +ve & I_0 is -ve, power flow is always from load to source.

As load voltage $V_0 = (E + L\frac{di}{dt})$ is more than source voltage, type-B chopper is also called step-up chopper.

First and second quadrant converter - (type-C)

This type-C chopper is a combination of type-A & type-B chopper. The o/p voltage V_0 is always +ve because of the presence of FD across the load. The load current is either +ve or -ve as shown below.

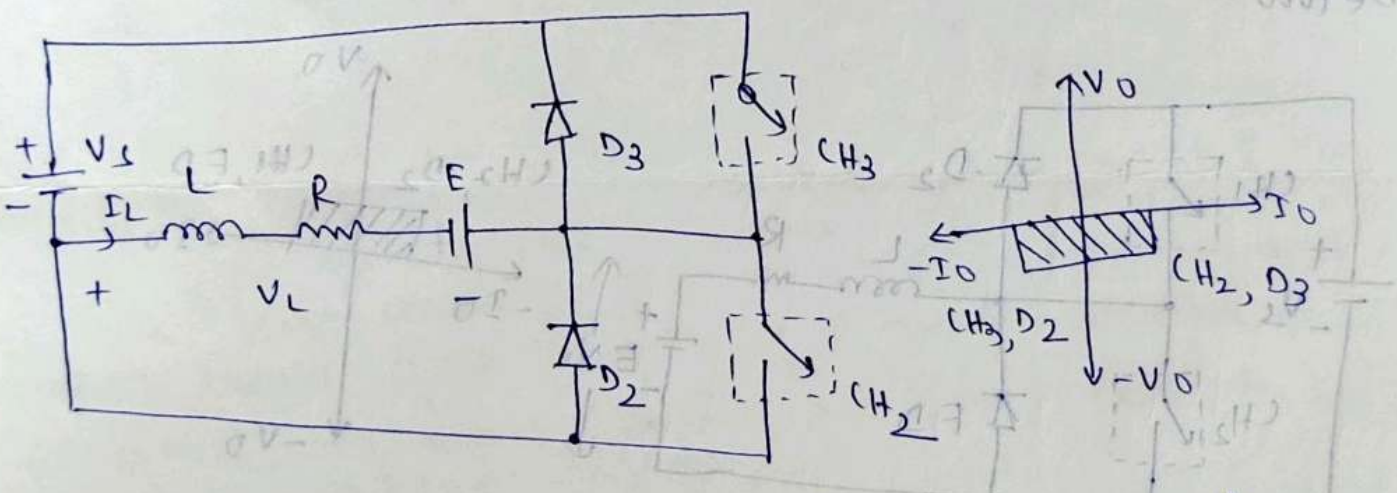


In this type of chopper power flow may be from source to load (first quadrant) or from load to source (second quadrant). The two switches are not fired together otherwise it would lead to short ckt of the source. This type of chopper is generally used for motoring and regenerative braking of dc motor.

In the first quadrant operation CH_1 or FD conducts. During ON period CH_1 conducts and during OFF period FD conducts.

→ In the second quadrant operation CH_2 or D_2 conducts. During ON period CH_2 conducts and during OFF period D_2 conducts. Here the current direction is opposite to the reference current direction, the current is -ve, o/p voltage is +ve and the power flow is -ve i.e. power flow from load to source.

Third and fourth quadrant converter:



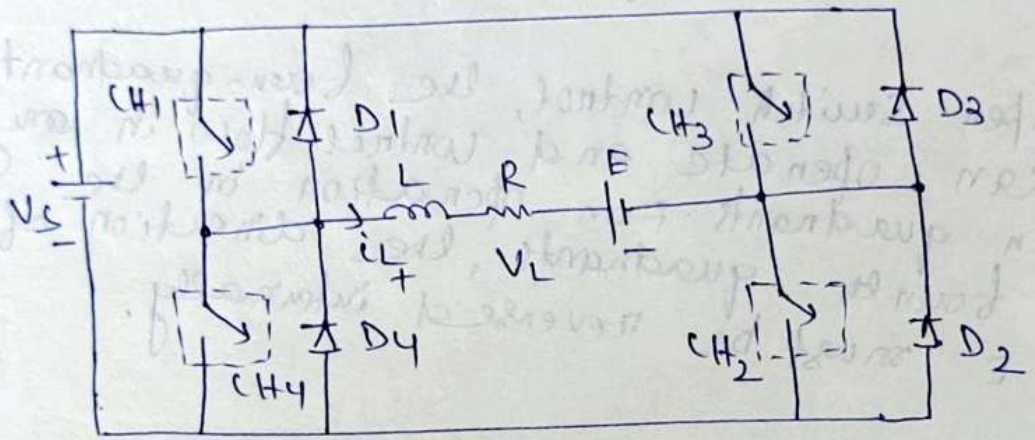
→ Here load voltage is always -ve. The load current is either +ve or -ve.

Here CH_3 and D_2 operate to yield both a -ve voltage and a load current. when CH_3 is ON, a -ve current flows through the load. when CH_3 is OFF, the load current freewheels through diode D_2.

→ CH_2 & D_3 operate to yield a -ve voltage and a +ve load current. when CH_3 is ON, a +ve load current flows. when CH_2 is OFF, the load current

free wheels through D3. It is important that the polarity of E must be reversed for this ckt to yield a -ve voltage and a +ve current. This a -ve two-quadrant converter. This converter can also operate as a rectifier or as an inverter.

Four-quadrant converter.



Here the load current is either +ve or -ve and the load voltage is also either +ve or -ve.
→ one first and second quadrant converter and one third and fourth quadrant converter can be combined to form the four-quadrant converter as shown in above figure.

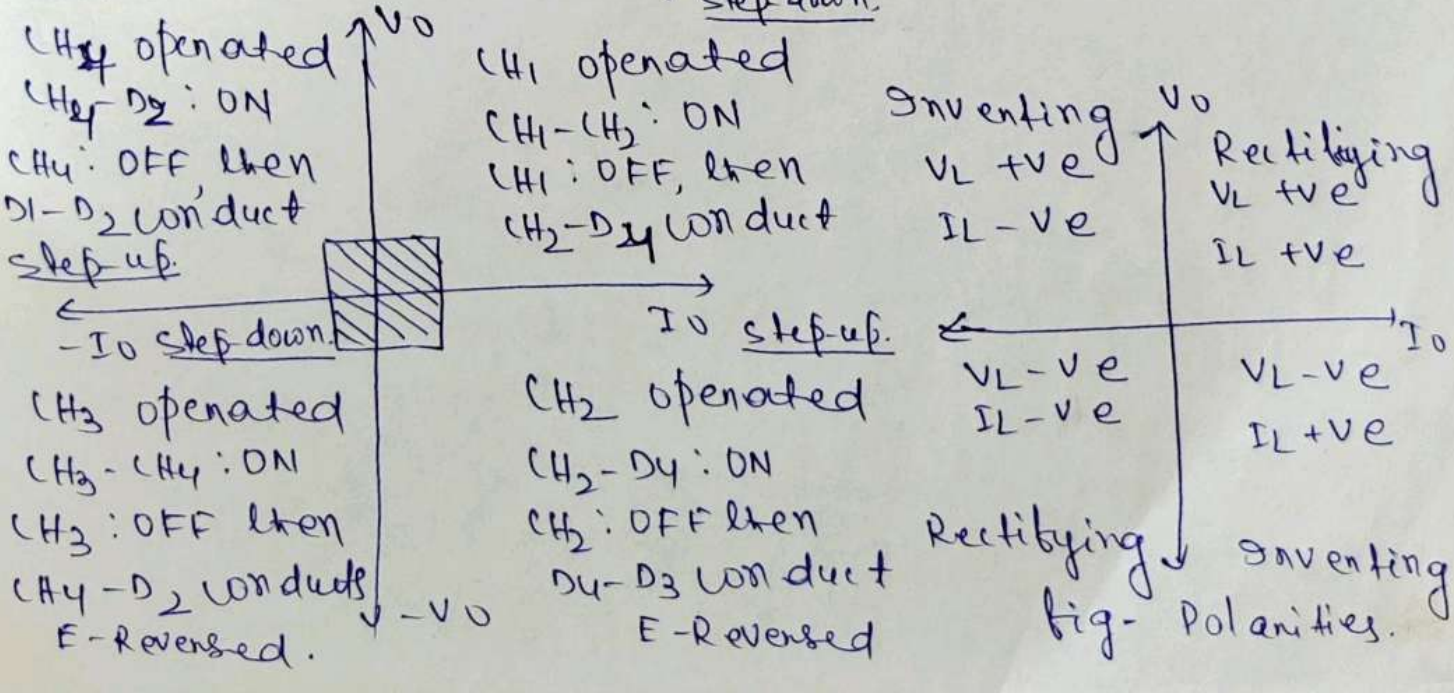
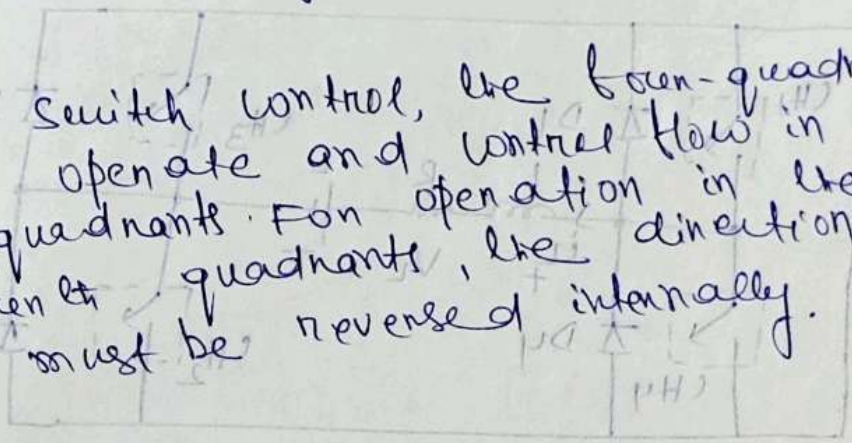


fig- Polarities.

This converter forms the basis for the single-phase full-bridge inverter.

For an inductive load with an emf (E) such that as a dc motor, the four-quadrant converter can control the power flow and the motor speed in the forward direction (v_L +ve & i_L +ve), forward regenerative braking (v_L +ve & i_L -ve), reverse direction (v_L -ve & i_L -ve) and reverse regenerative braking (v_L -ve & i_L -ve).

→ with proper switch control, the four-quadrant converter can operate and control flow in any of the four quadrants. For operation in the third and fourth quadrants, the direction of load emf E must be reversed internally.



DC to AC converters (Inverters)

A device that converts dc power into a c power at desired op voltage and frequency is called an inverters.

Inversion :- Inversion is a process of converting DC power to A.C. power.

Phase-controlled converters, when operated in the inverter mode, are called line-commutated inverters.

Application.

1. Induction heating
2. HVDC transmission lines
3. variable speed AC motor drives
4. Uninterruptible power supply (UPS)

PWM Inverter. The variable o/p voltage of inverter can be obtained by PWM techniques, is known as PWM inverter.

1-ϕ bridge Inverter. Bridge inverters are very popular and commonly used in dc-ac conversion because they can be easily extended for multi-phase operation, pulse-width modulation etc. Also the o/p transformer is not essential in bridge inverters. 1-ϕ bridge inverters are of two types, namely

(i) Single-phase half-bridge inverter
(ii) Single-phase full-bridge inverter.

1-φ half-bridge Inverter.

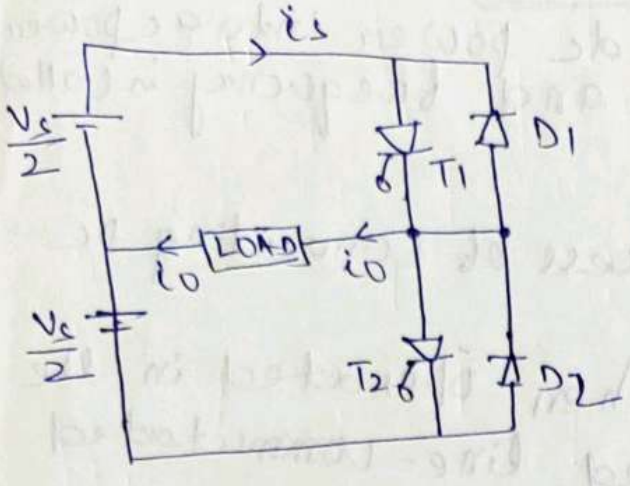


Fig.(a)

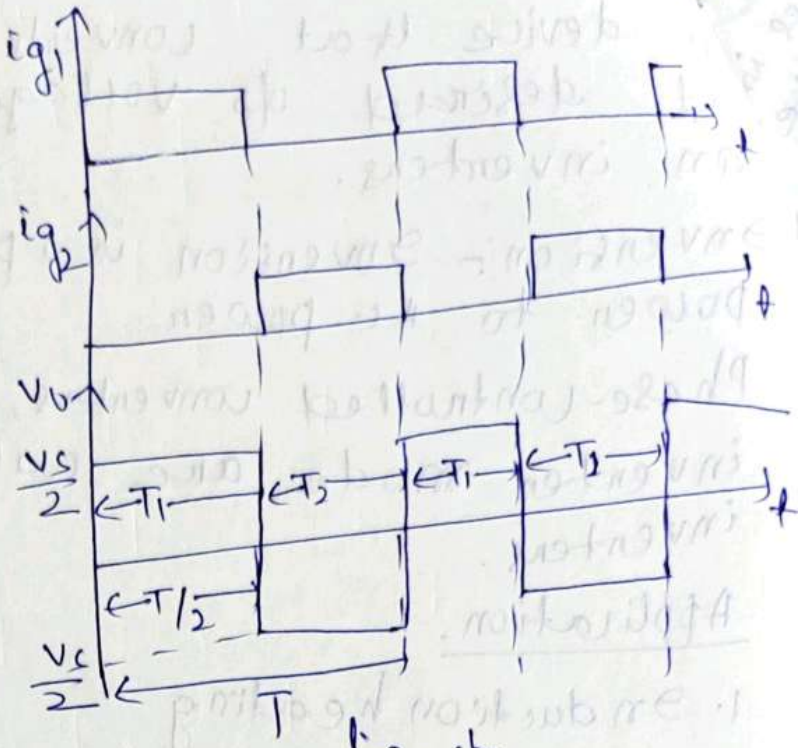


fig. (b)

It uses two sources and two switches. Diodes D_1 and D_2 provide freewheeling operation and are needed only if the load is inductive or capacitive. For purely resistive loads D_1 & D_2 don't come into operation.

→ The o/p voltages and gate signals for resistive load is shown in fig. (b).

SCR T_1 conducts for a period of $\frac{T}{2}$. SCR T_1 is commutated at $\frac{T}{2}$, then SCR T_2 is triggen. SCR T_2 is commutated at $t = T$. This process is repeated to obtain a continuous rectangular wave. It must be ensure that T_1 & T_2 are not triggered simultaneously. The voltage across the load is alternating one whose amplitude is given as $\frac{V_s}{2}$ with a frequency $f_0 = \frac{1}{T}$ Hz.

rms o/p voltage (V_{or})

$$V_{or} = \left[\frac{1}{T/2}\int_0^{T/2}\left(\frac{V_s}{2}\right)^2 dt\right]^{1/2} = \frac{V_s}{2}$$

Rms o/p current I_{rms}

$$I_{rms} = \frac{V_s}{2R}$$

Full bridge inverter.

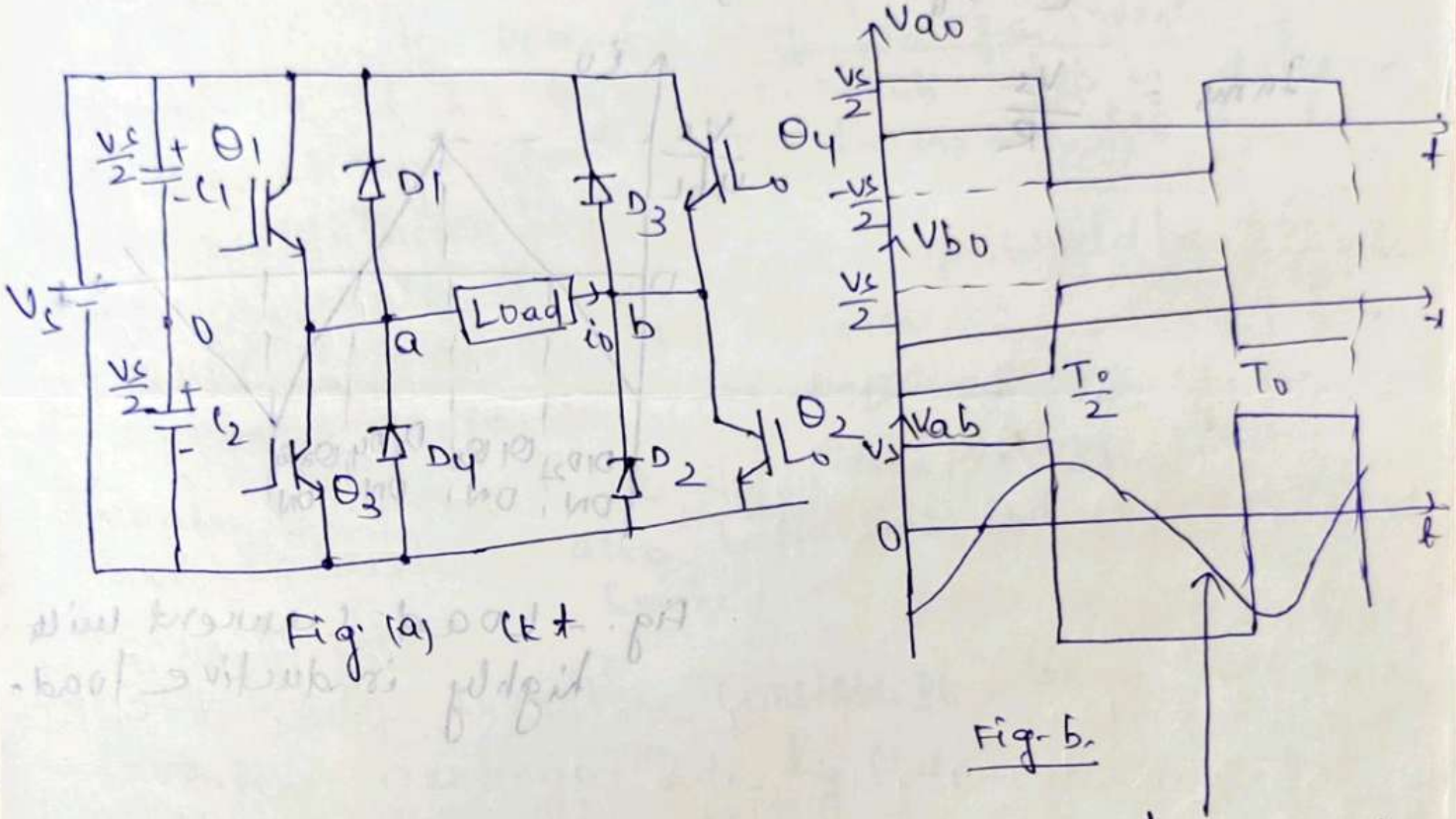


Fig (a) Circuit

Fig-b.

fundamental current, i_{o1}

A 1-Φ full bridge voltage source inverter (VSI) is shown above. It consists of four switches. When transistor Q_1 & Q_2 are turned on simultaneously, the input voltage V_s appears across the load. If transistor Q_3 & Q_4 are turned on at the same time, the voltage across the load is reversed & is $-V_s$. The waveform for the o/p

voltage is shaon in fig. (b)

→ In this inverter no. of switches & diodes twice that of half bridge inverter, but the amplitude of o/p voltage & power is double as compared to half bridge inverter.

The rms o/p voltage

$$V_{or} = \left[\frac{1}{T/2}\int_0^{T/2} V_s^2 \cdot dt\right]^{1/2} = V_s$$

$$I_{rms} = \frac{V_s}{R}$$

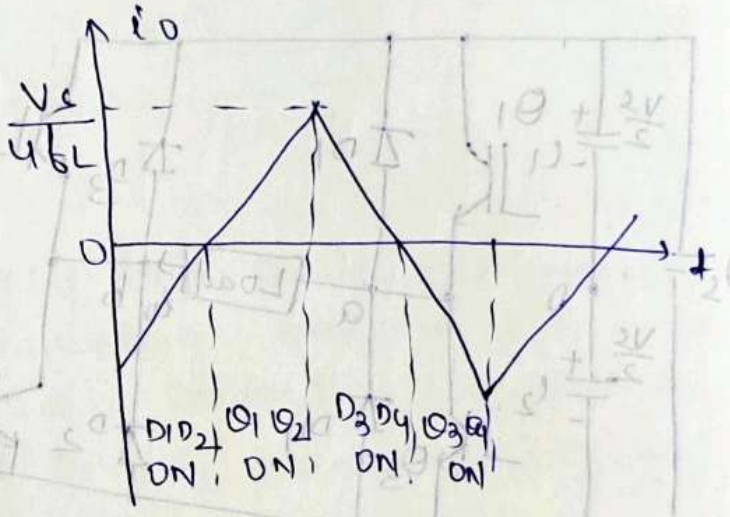


Fig. - Load current with highly inductive load.

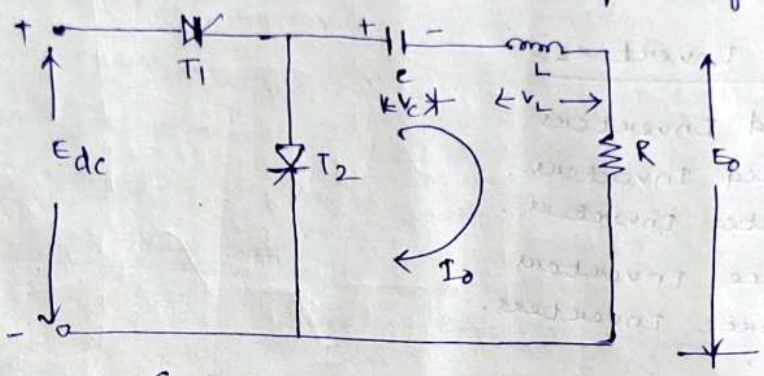
→ Inverters are also classified, depending upon the connection of commutating components with the main circuit.

(a) Series Inverters
(b) Parallel Inverters
(c) Bridge Inverters → 1φ half bridge Inverters.
→ 1φ full bridge Inverters.

Series Inverters

→ Series Inverters are those Inverters in which the commutating elements L and C are connected in series with the load. This circuit consists a series R-L-C resonant circuit. Produced high O/P freq range 200 Hz - 100 KHz.

→



Construction / (circuit Description)

→ It consists of two thyristors which are used to produce the +ve and -ve half cycles respectively in the o/p. The commutating elements L and C are connected in series with the load. The value of L & C are selected that they form an under damped circuit, to produced the required oscillations.

⇒ $R^2 < \frac{4L}{C}$ the above condition full filled, where the values of L and C are selected by satisfying the above relation.

working :-

Mode-1

→ Th T_1 is triggered by giving a gate signal to it, Th T_1 start conducting. As results current flowing through R-L-C, and capacitor gets charged up to Ec. Load current flows through the path $E_{dc}^{+} - T_1 - C - L - R - E_{dc}^{-}$

→ The load current produced is of alternating in nature which is due to the underdamped ckt formed by commutating elements.

When the load current reaches its peak value, the voltage across the capacitor is given as E_{dc}.

→ E_c is the initial voltage across the capacitor when T_1 triggered. When the load current reaches a zero value, SCR T_1 gets turned off.

Mode-2

→ During this Mode, the load current remains constant for a sufficient period of a time before SCR T_2 is triggered. It is necessary to maintain load current constant in order to prevent dead short circuit of supply.

⇒ Which may be caused when both the SCRs are in the conducting Mode. During this Mode, both T_1 and T_2 are in off state. Here the capacitor Vtg remains constant.

Mode-3

→ When T_2 is triggered, it start conducting and the capacitor 'c' gets discharged through it. Here the load current direction is opposite to that of the load current direction of Mode(i)

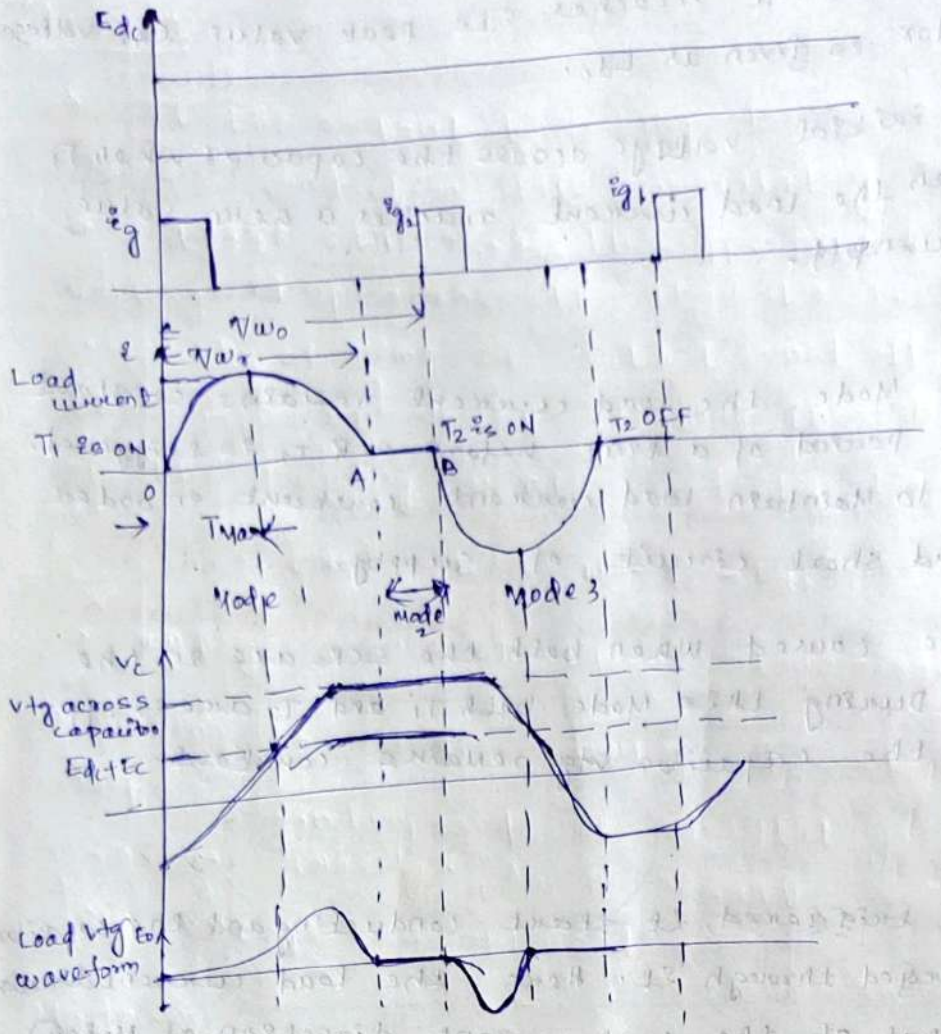
→ The load current flows through the path.

$$c^+ - T_2 - R - L - c^-$$

→ This current builds up to the negative maximum and then reaches a zero value. When the load current reaches a zero value, T_2 get turned off. Depending upon the values of R, L and c the voltage across the capacitor gets reversed to some value.

→ After some time, again T_1 triggered and the above process is Repeated. Hence alternating o/p which is of sinusoidal in nature is obtained.

→ The current has been drawn from supply for +ve alternation of A.C o/p whereas it is drawn from capacitor, for -ve alternation of A.C o/p.



CONS:-

→ Power Flow From the dc Supply is discontinuous.

→ The dc Supply will have a high peak current and hence contains harmonics.

→ If proper time delay is not ensured b/w the turn off process of thyristor T_1 and turn on process of Thyristor T_2, short circuit of Supply voltage takes place.

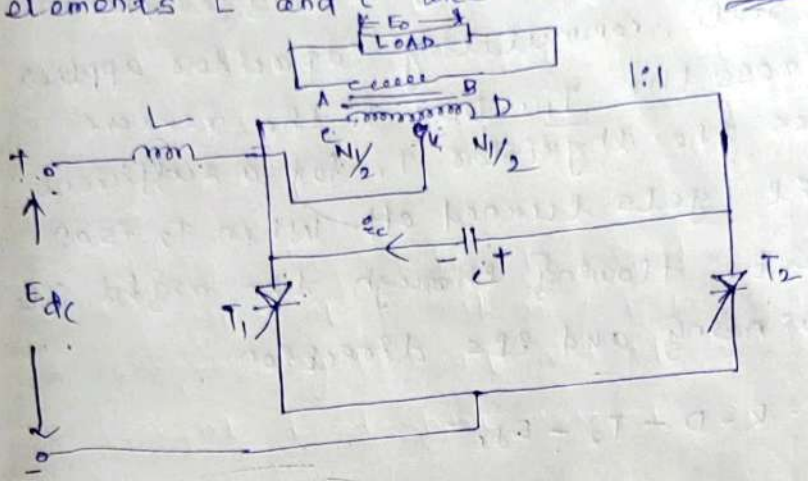
→ As the current drawn from dc source is discontinuous, more ripples are present in it.

→ Load ckt parameters determine the peak amplitude and duration of load current which results the poor output regulation of an inverter.

→ The ratings of the commutating elements Must be high because these components carry load current continuously and the capacitor supplies the load current in every alternate half cycle.

Parallel Inverter:-

→ Parallel inverter are those inverters where the commutating elements L and C are connected across the load.



Construction / circuit Description:-

→ It consists of two thyristors T_1 & T_2 connected to the primary of the transformer. The capacitor is connected across load via T/F, hence it is known as parallel inverter.

→ The Function of L is to Make source current constant at t_0 and in order to prevent the instant discharge of capacitor 'c' whenever thyristor switching occurs. Parallel inverter is generally used to produce a square wave From the D.C source.

Mode-1

→ At the instant $t=0$, T_1 is turned on. The current starts flowing through the Leftside of the primary winding, and its direction is given by

$$E_{dc}^{+} - L - K - C - T_1 - E_{dc}^{-}$$

→ As a result, supply voltage E_{dc} appears across the Left Half of the T/F primary. Bcz of the closely coupled coil and same number of turns the voltage across the DK is also E_{dc}. By the dot convention, the voltage across KC = $+E_{dc}$ voltage across DK = E_{dc}.

→ on the secondary side of the T/F $2E_{dc}$ is induced. Hence the capacitor gets charged to a voltage of $2E_{dc}$ with the polarity.

Mode-2

→ At the instant $t = T_0$, Thyristor T_2 is triggered when T_2 is conduction state, commutating capacitor applies a voltage $2E_{dc}$ across the T_1. Due to the reverse voltage drop across the thyristor T_1 for a sufficient amount of time, it gets turned off. When T_2 is on the current starts flowing through the right side of the primary winding and its direction

$$E_{dc}^{+} - L - K - D - T_2 - E_{dc}^{-}$$

→ voltage across $KD = E_{dc}$, voltage across $CK = E_{dc}$.

→ During this Mode, a voltage of $2E_{dc}$ appears across T/F Secondary and the commutating capacitor has reverse polarity. As a result, -ve cycle of the O/P voltage is obtained.

Mode-3

→ At the instant, $t = 2T_0$, Thyristor T_1 triggered and hence T_2 gets Turned off by above process. Hence this way if triggering pulses are given at regular intervals of time to the alternate thyristor, approximately rectangular voltage waveform may be obtained.

Probs:-

→ The circuit so simple.

→ Small in size and less expensive

→ It employs complementary voltage commutation.

CONS:-

→ Whenever the circuit is operated at low frequencies. T/F 's core get saturated which is an undesirable result. This is because, at low frequencies each thyristor conducts for higher duration which saturates the T/F's core.

Battery Chargers

It is necessary to charge a battery to restore it's fully charged condition. During charging a current is sent through the battery in a direction opposite to that at when the battery is being used. The charging current is generally obtained from bridge rectifier. The ckt should give an indication that the charging is over, in addition provision for trickle charging should also exist.

→ Trickle charging means charging at a slow rate to keep the battery in fully charged condition. The battery is permanently connected to the load as well as to the charger & is continuously charged at a slow rate. Generally the battery charger has a 'quick charge' setting and 'trickle charge' setting. After a heavy discharge, the charger is put on 'quick charge' to charge the battery quickly. After quick charging is over, the battery is again put on trickle charge setting. A battery charging ckt which has arrangent for both quick charge and trickle charge is shown in next page. For charging a 12V battery the transformer turns ratio N_1/N_2 is 11.5 : 1. The bridge rectifier converts low voltage ac to dc. This rectifier ckt generally uses diodes because charging current requirement is small. Diode D_5 triggers the thyristor (SCR) into conduction and the charging current flows through

thyristor into the battery. The voltage to which the battery is to be charged can be adjusted by adjusting resistance R6. The resistance R_1 is high power resistance because it carries full charging current.

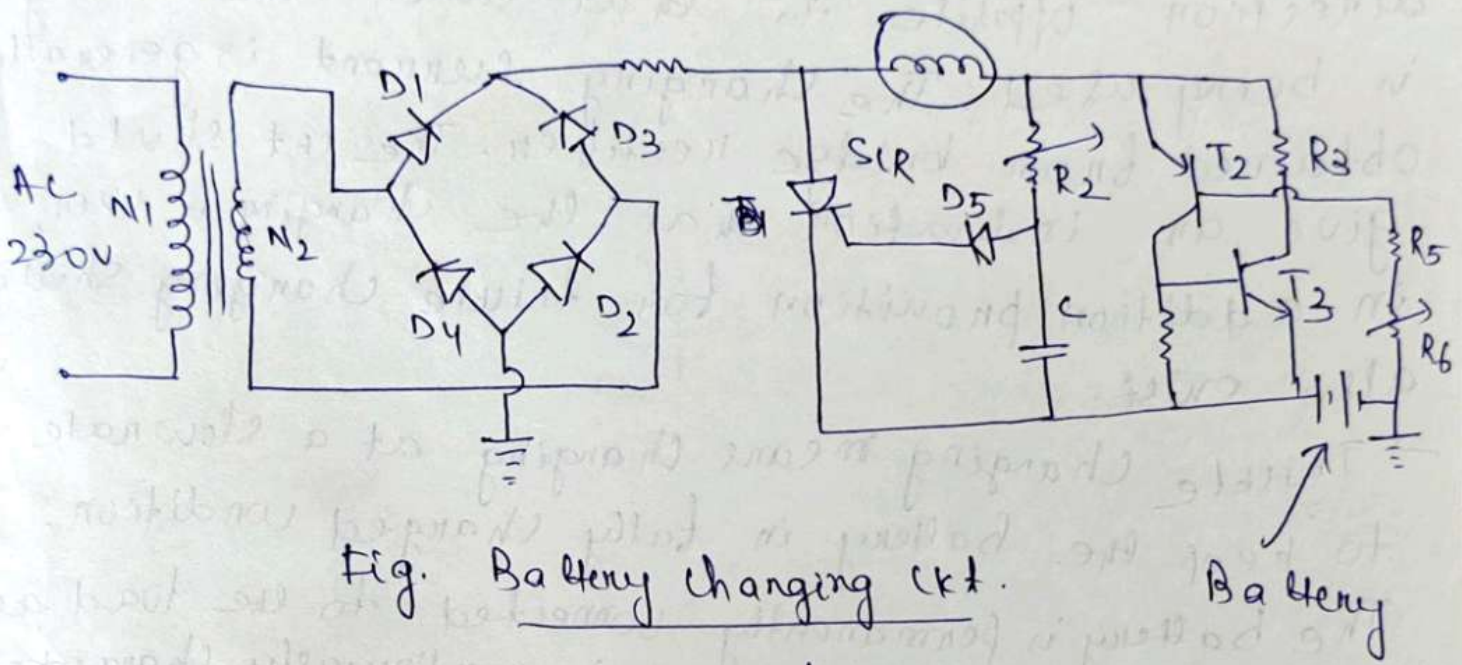


Fig. Battery changing ckt.

when the battery becomes fully charged, transistors T_1 and T_2 starts conducting. The capacitor C discharge through the low impedance path through T_1 and T_2. This action commutates thyristor into non-conducting mode.

After the battery is charged, a small current continues to flow through the neon lamp which starts glowing. This small current is the trickle charge current for the battery.

Uninterruptible Power Supply (UPS)

Uninterruptible Power supply means there is no interruption (failure) of power supply to the device or equipment on the failure of Grid (mains) supply.

The UPS converts the bad quality commercial supply into good quality power supply of constant voltage and frequency. Normally the critical loads requires UPS.

Critical loads are:

1. Hospitals (ICU)
2. Airline and Railway reservation system.
3. Computer system.
4. Process control in plants.

The basic block diagram of UPS is shown in fig (a)

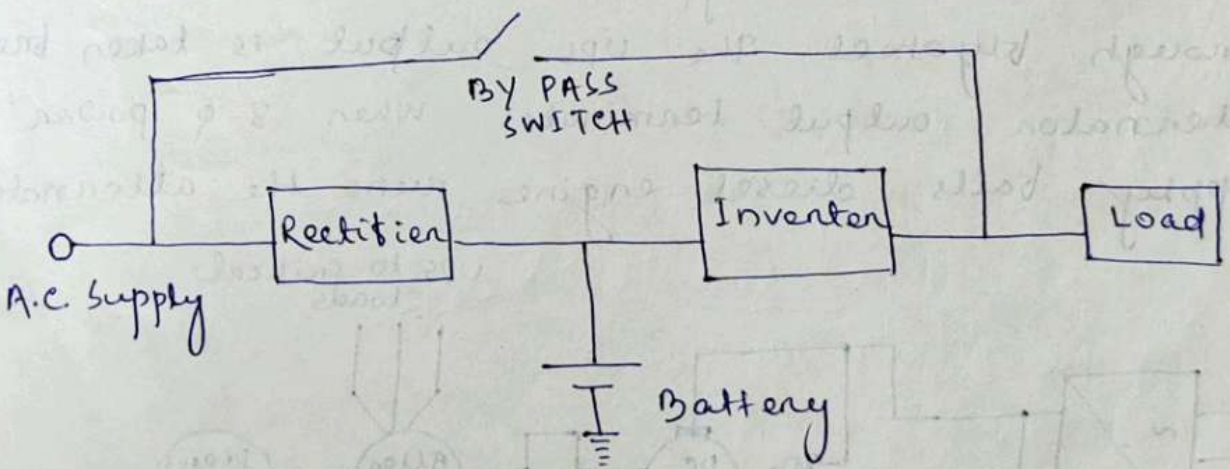
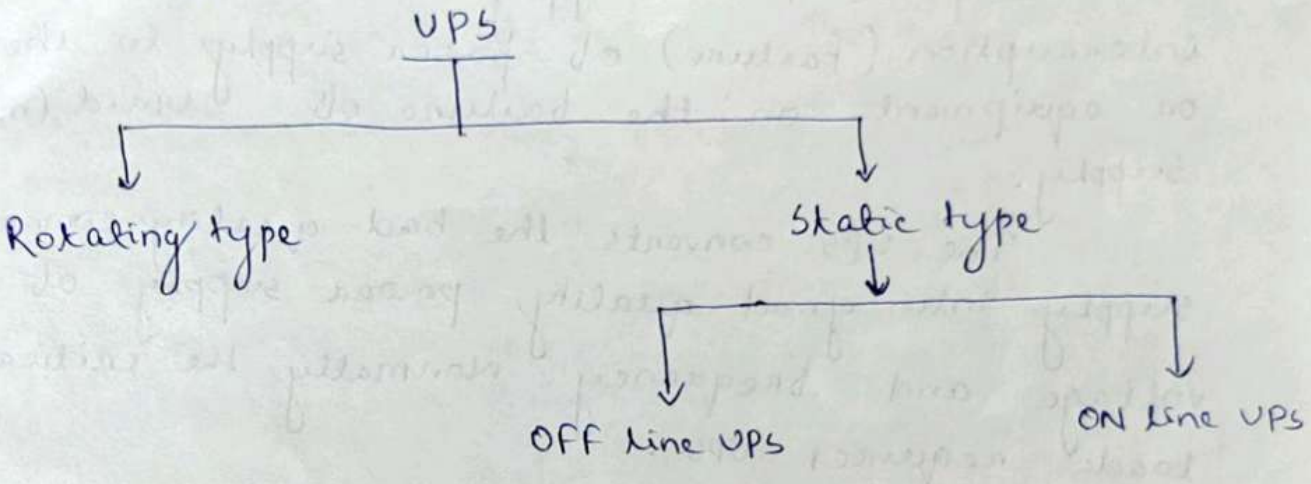


Fig (a)

The Rectifier convert AC into DC. This DC voltage charges the battery. The battery voltage is the dc input to inverter. When the AC supply fails, the DC input to the inverter is given by the battery. The bypass switch is closed in case of

failure of Rectifier and battery.

Presently the UPS can be classified as follows:



Rotating type UPS:

Earlier UPS systems are based on this type. The arrangement is shown in fig (b). In this arrangement 3-ϕ a.c. supply is converted to d.c. by means of rectifier and charges a battery bank and feeds the d.c motor. The shaft of the dc motor is supplied with alternator shaft through flywheel. The UPS output is taken from alternator output terminals. When 3-ϕ power supply fails, diesel engine runs the alternator.

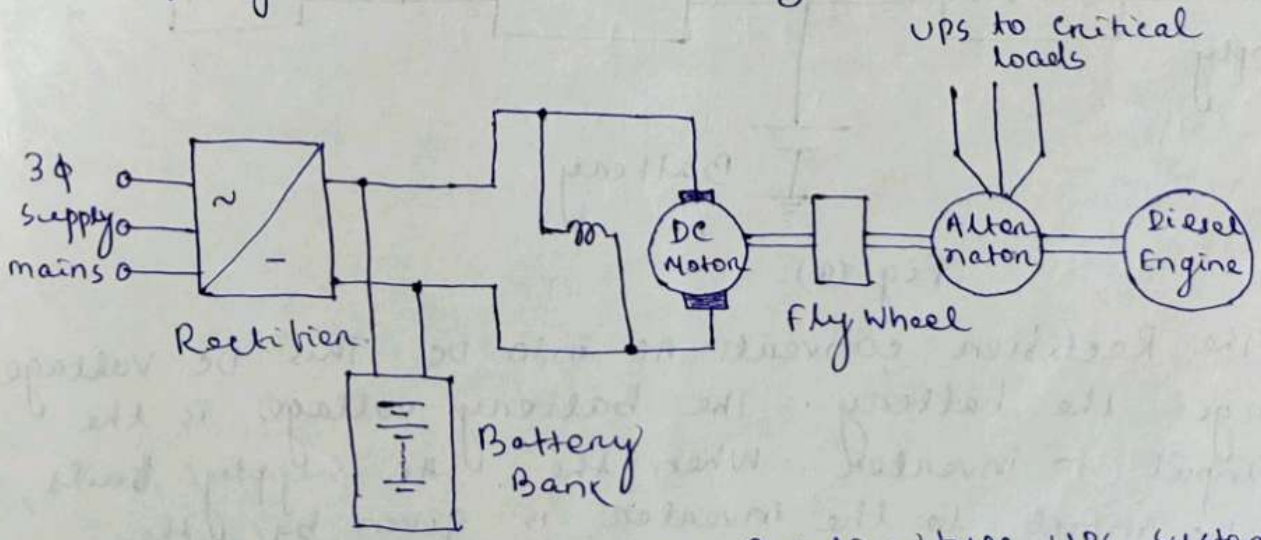


Fig-(b) Rotating type UPS system based on dc motor / alternator set

OFF Line UPS :

The configuration of OFF line UPS is shown in fig-(c). In this type the inverter is normally in off state. The load is fed from the AC mains directly through static switches. When the AC mains supply is not available, the inverter section is automatically ON and fed the load through a static switch. The static switch takes around 5ms to connect the load to inverter. This type UPS is cheaper than ON line UPS.

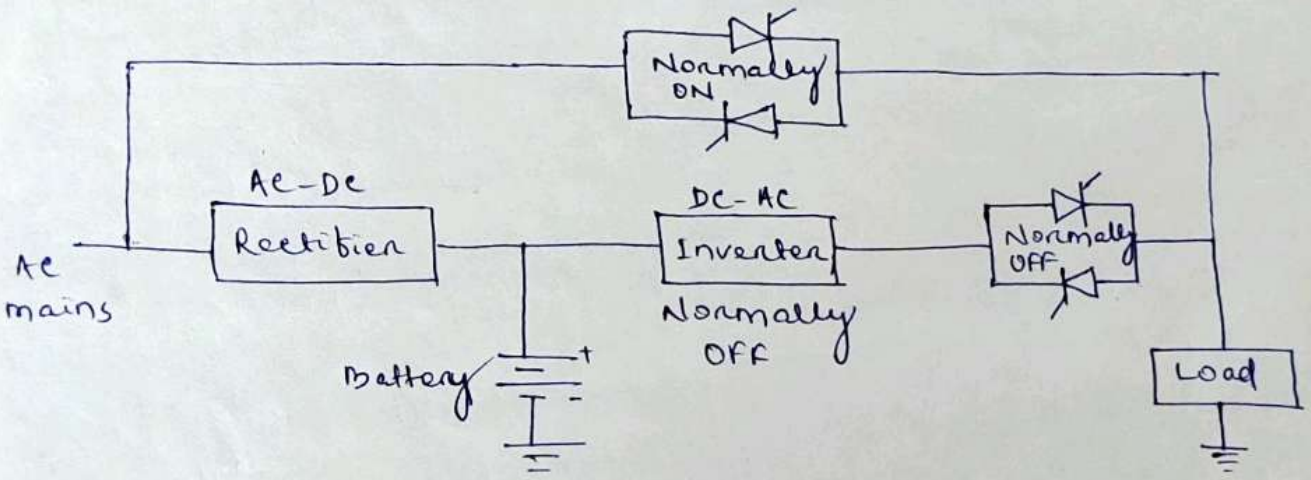


Fig-(c) OFF line UPS.

ON Line UPS :

The configuration of on line UPS is shown in fig-(d). In this type the inverter section is normally on and the load is fed by the inverter through a static switch. The advantage of this type is the output of inverter can be controlled, and constant voltage constant frequency at the output can be maintained. If there is some fault occurs in the inverter, the load is fed through the bypass static switch as shown in the figure.

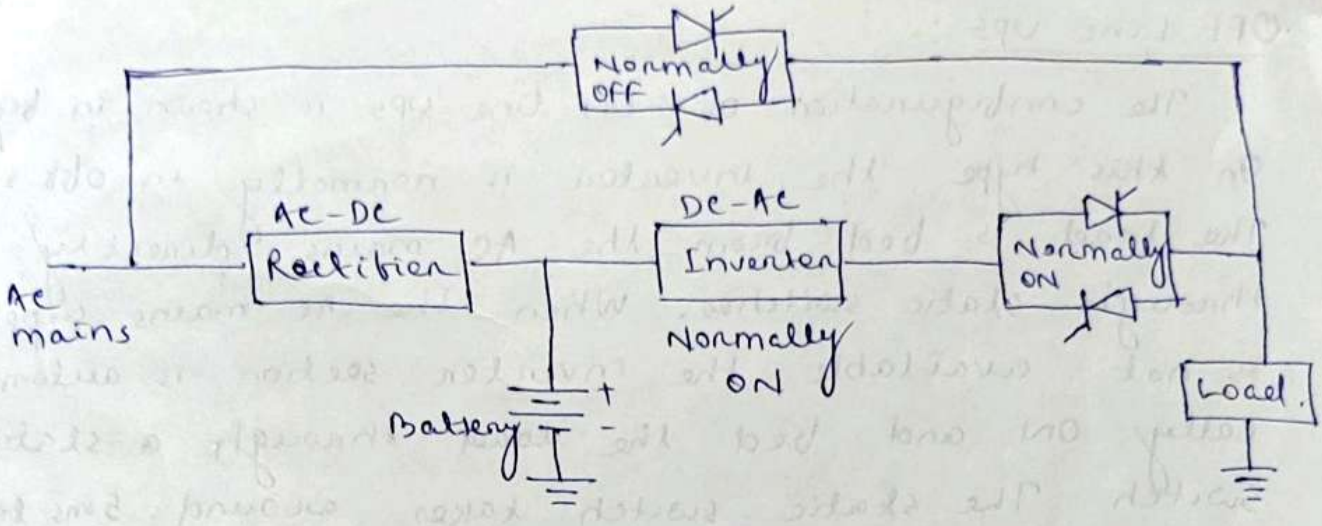
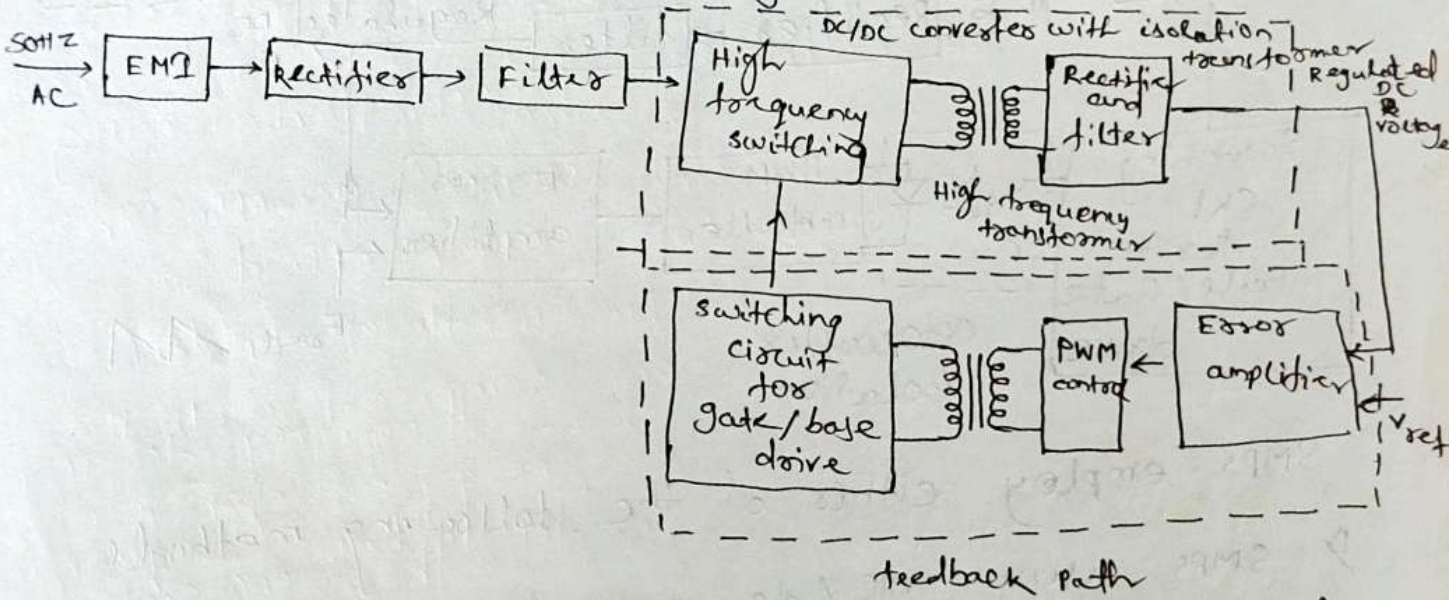


Fig.-(d) On line UPS

SMPS (switch mode power supply) →

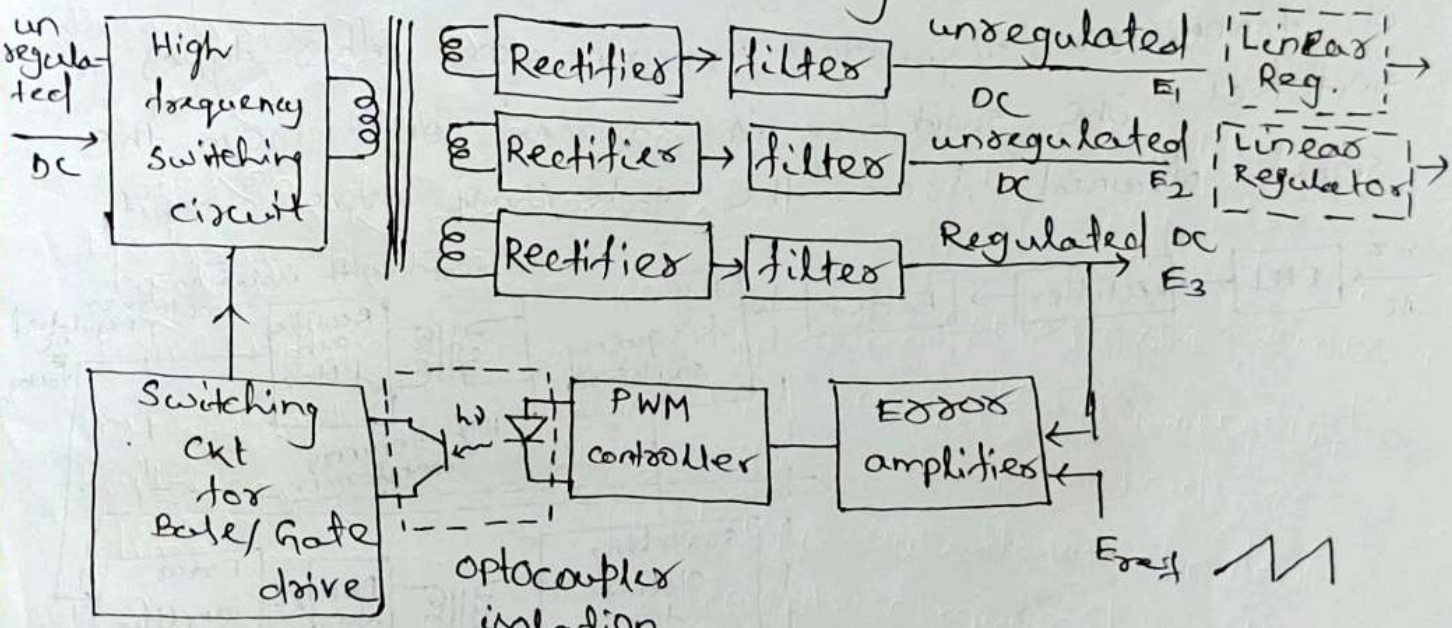
The block diagram of SMPS is shown in fig. In the diagram the EMI filter prevents conducted EMI. The a.c voltage then rectified by rectifier and then filtered. The unregulated dc is then fed to dc/dc converter block. In the dc/dc converter block the dc is converted to high frequency by means of a high frequency switching circuit that comprises of transistors/ thyristors / MOSFETs or other types of switches. The switching is carried out from the signal obtained from the gate/base drive circuit



The high frequency ac is applied to the primary of a high frequency isolation transformer. The output of isolating transformer is rectified and filtered to produce an output E_0. The output of the d.c supply is regulated using a feedback control circuit that employs PWM controller. The control voltage is compared with a sawtooth voltage waveform at the switch frequency.

The electrical isolation in the feedback loop is provided by means of an optocoupler or through an isolation transformer.

For multiple outputs the outputs may be electrically isolated from one another using isolation transformer. The block diagram of multiple output SMPS is shown in figure.



SMPS employ either of the following methods.

1) SMPS using dc/dc converter
2) SMPS using resonant type converters that employ zero voltage and/or zero current switches.

Advantages →

→ The switching regulator employ devices (BJT, Thyristor, MOSFET) operates as switches.

A switch is either ON or OFF. Since the switches do not operate in the active region, power loss that would have occured had they operated in the active region is substantially reduced. This means a good energy efficiency is achieved.

→ Switching mode power supplies need high frequency isolation transformer.

Disadvantage →

More EMI is produced. Proper steps to be taken to prevent electromagnetic interference.

Programmable logic controllers (R. Dick Morley, 1969)

5:1 Introduction:-

- A PLC (Programmable logic controller) is a device that was invented to replace the necessary sequential relay circuits for Machine control.
- The PLC works by looking at its inputs and depending upon their state, turning on/off outputs. The user enters a program, usually via software, that gives the desired results.

PLC Example:-

- Let's assume that when a switch turns on we want to turn a solenoid on for 5 seconds and then turn it off regardless of how long the switch is on for.
- We can do this with a simple external timer. But what if the process included 10 switches and solenoids? we would need 10 external timers. What if the process also needed to count how many times the switches individually turned on? we need a lot of external counters.

PLC Need:-

→ The bigger the process the more is need for a PLC.

→ Simply program the PLC to count its inputs and turn the solenoids on for the specified time.

→ The primary reason for designing PLC was eliminating the large cost involved replacing the complicated relay based Machine control systems.

Inside PLC:-

→ The PLC Mainly consists of

- → A CPU
- → Memory Areas, and
- → Appropriate circuits to receive input/output data
- → We can actually consider the PLC to be a box full of hundreds or thousands of separate relays, counters, timers and data storage locations.

Definition and History of the PLC :-

→ A PLC is a user-friendly, microprocessor-based specialized computer that carries out control functions of many types and levels of complexity

→ Its purpose is to monitor crucial process parameters and adjust process operations accordingly.

→ Used extensively because the PLC
- Is easy to set up and program
- Behaves predictably
- Rugged lined.

→ It can be programmed (to a degree) controlled, and operated by a person unskilled in operating (programming) computers.

→ Essentially, a PLC's operator draws the lines and devices of ladder diagrams with a keyboard/mouse onto a display screen.

→ The resulting ladder diagram is converted into computer m/c language and run as a program.

Example :-

→ Allen - Bradley PLC 5.

→ Allen - Bradley SLC500.

→ Allen - Bradley Micrologix.

→ Allen - Bradley Picocontroller.

PLC Basics :-

- Some PLCs are :—
  → Integrated into a single unit (Picocontroller).
  → Whereas others are Modular (PLCs, SLC500)
  → The Micrologix Product lies somewhere b/w the PLCs and the picocontrollex.
- Integrated PLCs :—

Integrated PLCs are sometimes called brick PLCs because of their small size

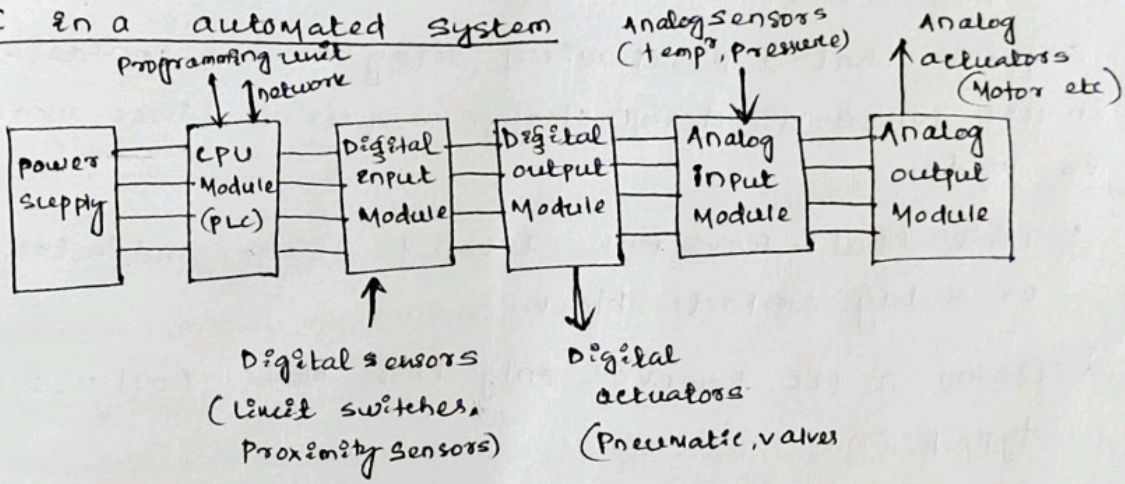
→ These PLCs because have embedded I/O (i.e the I/O is a part of the same unit as the controller itself.

→ Modular PLCs have extended I/O.

components in a PLC system

- CPU Module, containing the processor and memory
- Input and output Modules, to allow the PLC to read sensors and control actuators.
  → A wide variety of types are available
- Power supply for the PLC, and often sensors and low power actuators connected to I/O Modules
- A rack or bus so the PLC can exchange data with I/O Modules.

PLC in a automated system



5.2 (*) PLC Advantages

(a) Flexibility

→ In the past, each different electronically controlled production machine required its own controller, so machine might require 15 different controllers.

→ Now it is possible to use just one model of a PLC to run any one of the 15 machines.

→ Furthermore, you would probably need fewer than 15 controllers, because one PLC can easily run many machines.

→ Each of the 15 machines under PLC control would have its own distinct Program (or a portion of one running program)

(b) Implementing changes and correcting Errors:-

→ With a wired relay-type panel, any program alterations require time for rewiring of panels and devices.

→ When a PLC programming circuit or sequence design change is made, the PLC program can be changed from a keyboard sequence in a matter of minutes.

→ No rewiring is required for a PLC-controlled system.

→ Also, if a programming error has to be corrected in a PLC control ladder diagram, a change can be typed in quickly.

(c) Large Quantities of contacts:-

→ The PLC has a large number of contacts for each coil available in its programming.

→ Suppose that a panel-wired relay has four contacts and all are in use when a design change requiring three more contacts is made.

- Time would have to be taken to procure and install a new relay or relay contact block.

→ Using a PLC, however, only three more contacts would be typed in.

- contacts are now a "software" component.

(d) Lower cost:-

→ Increased technology makes it possible to condense more functions into smaller and less expensive packages.

→ Now you can purchase a PLC with numerous relays, timers, and counters, a sequencer, and other functions for a few hundred dollars.

(e) Pilot Running:-

→ A PLC programmed circuit can be evaluated in the lab. The program can be typed in, tested, observed, and modified if needed, saving valuable factory time.

(f) Visual observation:-

→ A PLC circuit's operation can be seen during operation directly on a CRT screen.

→ The operation or mis-operation of a ckt can be observed as it happens.

→ Logic paths light up on the screen as they are energized.

→ Troubleshooting can be more quickly during visual observation.

(g) Ladder or Boolean Programming Method:-

→ The PLC Programming can be accomplished in the ladder mode by an engineer, electrician or possibly a technician.

→ Alternatively, a PLC programmer who works in digital or Boolean control systems can also easily perform PLC Programming.

(h) Reliability and Maintainability:-

→ Solid-state devices are more reliable, in general, than mechanical systems or relays and timers. consequently, the control system maintenance costs are low and downtime is minimal.

(i) Documentation:-

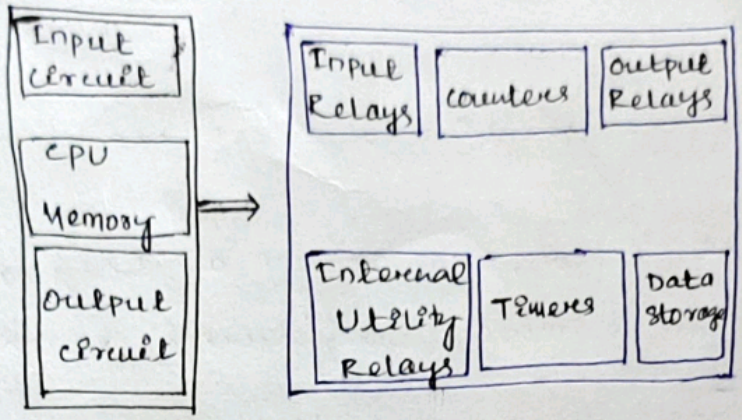
→ An immediate printout of the true PLC circuit is available in minutes, if required.

→ There is no need to look for the blueprint of the circuit in remote files.

→ The PLC prints out the actual circuit in operation at a given moment.

→ Often, the file prints for relay panels are not properly kept upto date

5:2 (various parts of PLC) BLOCK DIAGRAM:-



- Input Relays (contacts):-

→ These are connected to the outside world. They physically exist and receive signals from switches, sensors, etc. Typically they are not relays but rather they are transistors.

- Internal Utility Relays:-

→ These do not receive signals from the outside world nor do they physically exist. They are simulated relays and are what enables a PLC to eliminate external relays.

→ There are also some special relays that are dedicated to performing only one task. Some are always on while some are always off. Some are on only once during power-on and are typically used for initializing data that was stored.

- Counters:-

→ These again do not physically exist. They are simulated counters and they can be programmed to count pulses. Typically these counters can count up, down or both up and down.

- Timers:-

→ These also do not physically exist. They come in many varieties and increments. The most common type is on-delay type. others include off-delay and both retentive and non retentive types. Increments vary from 1ms through 1s.

- Output Relays (coils)

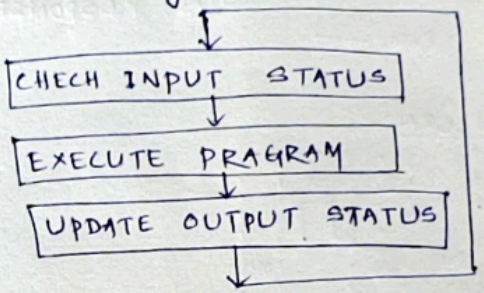
→ These are connected to the outside world. They physically exist and send on/off signals to solenoids, lights. They can be transistors relays, or triacs depending upon the model chosen.

- **Data Storage:-**

→ Typically there are registers assigned to simply store data. They are usually used as temporary storage for math or data manipulation. They can also typically be used to store data when power is removed from the PLC. Upon power-up they will still have the same contents as before power was removed.

PLC Operation:-

→ A PLC works by continually scanning a program, we can think of this scan cycle as consisting of 3 important steps.



→ **Step-1:- CHECH I/P Status:-**

→ First the PLC takes a look at each input to determine if it is on or off. In other words, is the sensor connected to the first input? How about the second i/p? How about the third ... it records this data into its memory to be used during the next step.

→ **Step- 2 - EXECUTE PRAGRAM:-**

→ Next the PLC executes program one instruction at a time. May be Program said that if the first input was on then it should turn on the first output. Since it already knows which inputs are ON/OFF from the previous step it will be able to decide whether the first o/p should be turned on based on the state of the ~~first~~ first input. It will store the execution results ~~results~~ for use later during the next step.

→ **Step-3- UPDATE OUTPUT STATUS:-**

→ Finally the PLC updates the status of the outputs. It updates the o/p based on which inputs were on during the first step and the results of executing your program during the second step. Based on the example in step-2 it would now turn on the first o/p because the first i/p was on and your program said to turn on the first output when this condition is true.

After the third step the PLC goes back to step one and Repeats the steps continuously. one scan time is defined as the time it takes to execute the 3 steps listed above.

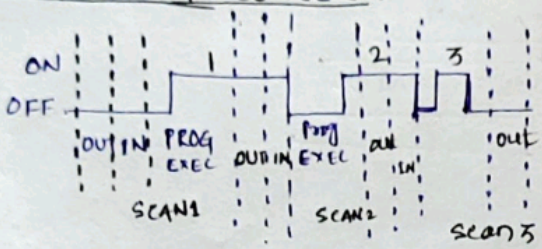
PLC - Response:-

→ The total response time of the PLC is Fact we have to consider when Purchasing a PLC.

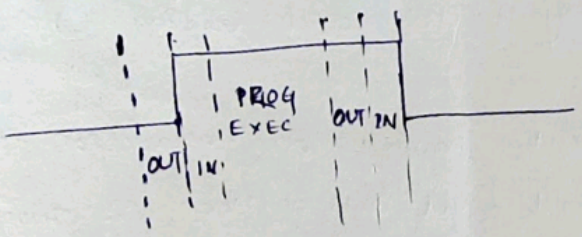
→ PLC takes a certain amount of time to react to changes. In many applications speed is not a concern, in others though.....

→ Input Response TIME
PROGRAM EXECUTION TIME
OUTPUT RESPONSE TIME
= TOTAL RESPONSE TIME

PLC - RESPONSE TIME CONCERN:-



- Input 1 is not seen until scan 2.
- Input 2 is not seen until scan 3.
- Input 3 never seen by PLC.



→ To Avoid this we say that the i/p should be ON for at least 1 input delay time + one scan time.

→ But what if it was not possible for the input to be on this long? Then the PLC doesn't see the input turn on.

PULSE STRETCH FUNCTION:-

→ This Function extends the length of the i/p signal until the PLC looks at the inputs during the next scan (it stretches the duration of the Pulse).