

DISCIPLINE – ELECTRICAL ENGG	SEMESTER 5TH	NAME OF THE TEACHING FACULTY- NIHARIKA SETHY, LECT(ETC.)	
SUB-DEMP	No Of Days Per Week Class Alloted- 5	SEMESTER FROM 9.09.2020 TO 03.03.2021 NO OF WEEK – 16 WEEKS	
WEEK	CLASS DAY	THEORY	STATUS
1 <sup>ST</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5th	Binary, Octal, Hexadecimal number systems and compare with Decimal system. Binary addition, subtraction, Multiplication and Division. 1's complement and 2's complement numbers for a binary number Subtraction of binary numbers in 2's complement method.	Completed
2 <sup>nd</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5th	Use of weighted and Un-weighted & codes Write Binary equivalent number for a, number in 8421 Excess-3 and Gray Code and vice-versa. Importance of parity Bit Logic Gates: AND, OR, NOT with truth table NAND, NOR and EX-OR gates with truth table	-do-
3 <sup>RD</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5th	Realize AND, OR, NOT operations using NAND, NOR gates. Different postulates and De-Morgan's theorems Boolean algebra. Use Of Boolean Algebra For Simplification Of Logic Expression DO	-do-

4 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5 <sup>TH</sup>	Use Of Boolean Algebra For Simplification Of Logic Expression SOP And POS Logic Expression Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map. DO	
5 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5 <sup>TH</sup>	Give the concept of combinational logic circuits. Half adder circuit and verify its functionality using truth table. Realize a Half-adder using NAND gates only and NOR gates only. Full adder circuit and explain its operation with truth table IA EXAM	-do-
6 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day	Realize full-adder using two Half-adders and an OR – gate and write truth table Give the idea of Sequential logic circuits. State the necessity of clock and give the concept of level clocking and edge triggering	

	5th	Clocked SR flip flop with preset and clear inputs	
7 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5th	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table  JK flip flop using S-R flip-flop  Concept of race around condition and study of master slave JK flip flop  Class Test	
8 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5th	Give the truth tables of edge triggered D and T flip flops and draw their symbols.  Applications of flip flops.  Introduction of counter. Define modulus of a counter  4-bit asynchronous counter and its timing diagram.  DO	
9 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5th	Asynchronous decade counter,  4-bit synchronous counter  Distinguish between synchronous and asynchronous counters  State the need for a Register and list the four types of registers.  Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.	
10 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day 4 <sup>TH</sup> day 5th	Introduction to Microprocessors, Microcomputers  Architecture of Intel 8085A Microprocessor and description of each block  DO  Pin diagram and description of 8085A  DO	
11 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>ND</sup> day 3 <sup>RD</sup> day	Stack, Stack pointer & stack top Interrupts Opcode & Operand, DO	-do-

	4 <sup>th</sup> day 5 <sup>th</sup>		
12 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day	Differentiate between one byte, two byte & three byte instruction with example. Instruction set of 8085 example DO. Addressing mode . .	
13 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5 <sup>th</sup> day	CLASS TEST Fetch Cycle, Machine Cycle, Instruction Cycle, T-State Timing Diagram for memory read, memory write, I/O read, I/O write. Timing Diagram for 8085 instruction Counter and time delay Simple assembly language programming of 8085.	
14 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5 <sup>th</sup> day	DO Basic Interfacing Concepts, Memory mapping & I/O mapping Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 , DO Application using 8255:	
15 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5 <sup>th</sup> day	Seven segment LED display Square wave generator IA EXAM Traffic light Controller DO	
16 <sup>TH</sup> WEEK	1 <sup>ST</sup> day 2 <sup>nd</sup> day 3 <sup>rd</sup> day 4 <sup>th</sup> day 5 <sup>th</sup> day	ASSIGNMENT DOUBT CLEARING CLASS DO SEMESTER QUESTION DISCUSSION SEMESTER QUESTION DISCUSSION	

