Q1. The binary number 10101 is equivalent to decimal number ……..

1. 19
2. 12
3. 27
4. 21

Answer : 4

Q2. The universal gate is ……

1. NAND gate
2. OR gate
3. AND gate
4. None of the above

Answer : 1

Q3. The inverter is ……

1. NOT gate
2. OR gate
3. AND gate
4. None of the above

Answer : 1

Q4. The inputs of a NAND gate are connected together. The resulting circuit is …….

1. OR gate
2. AND gate
3. NOT gate
4. None of the above

Answer : 3

Q5. The NOR gate is OR gate followed by ……

1. AND gate
2. NAND gate

3. NOT gate
4. None of the above

Answer : 3

Q6. The NAND gate is AND gate followed by ……

1. NOT gate
2. OR gate
3. AND gate
4. None of the above

Answer : 1

Q7. Digital circuit can be made by the repeated use of ……

1. OR gates
2. NOT gates
3. NAND gates
4. None of the above

Answer : 3

Q8. The only function of NOT gate is to ……..

1. Stop signal
2. Invert input signal
3. Act as a universal gate
4. None of the above

Answer : 2

Q9. When an input signal 1 is applied to a NOT gate, the output is ……

1. 0
2. 1
3. Either 0 & 1
4. None of the above

Answer : 1

Q10. In Boolean algebra, the bar sign (-) indicates ……..

1. OR operation
2. AND operation
3. NOT operation

4. None of the above

Answer : 3

Q11. The resolution of an *n* bit DAC with a maximum input of 5 V is 5 mV. The value of *n* is …….

1. 8
2. 9
3. 10
4. 11

Answer : 3

Explanation:

$(5/2^N-1)1000 = 5$ or N = 10

Q12. 2's complement of binary number 0101 is ……..

1. 1011
2. 1111
3. 1101
4. 1110

Answer : 1

Explanation: 1's complement of 0101 is 1010 and 2's complement is 1010+1 = 1011.

Q13. An OR gate has 4 inputs. One input is high and the other three are low. The output is …….

1. Low
2. High
3. alternately high and low
4. may be high or low depending on relative magnitude of inputs

Answer : 2

Explanation: In OR any input high means high output.

Q14. Decimal number 10 is equal to binary number ……

1. 1110
2. 1010
3. 1001
4. 1000

Answer : 2

Explanation: 1010 = 8 + 2 = 10 in decimal.

Q15. Both OR and AND gates can have only two inputs.

1. True
2. False

Answer : 2

Explanation: Any number of inputs are possible.

Q16. A device which converts BCD to seven segments is called ……..

1. Encoder
2. Decoder
3. Multiplexer
4. None of these

Answer : 2

Explanation: Decoder converts binary/BCD to alphanumeric.

Q17. In 2's complement representation the number 11100101 represents the decimal number ……

1. +37
2. -31
3. +27
4. -27

Answer : 4

Explanation:

A = 11100101. Therefore $\bar{A}$ = 00011010 and A' = $\bar{A}$ + 1 = 00011011 = 16 + 8 + 2 + 1 = 27. Therefore A = -27.

Q18. A decade counter skips ……..

1. binary states 1000 to 1111
2. binary states 0000 to 0011
3. binary states 1010 to 1111
4. binary states 1111 to higher

Answer : 3

Explanation: A decade counter counts from 0 to 9. It has 4 flip-flops. The states skipped are 10 to 15 or 1010 to 1111.

Q19. BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are ……

1. *a, b, d*
2. *a, b, c*
3. all
4. *a, b, g, c, d*

Answer : 3

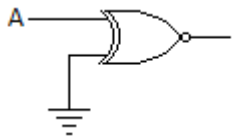
Explanation: 1000 equals decimal 8 Therefore all segments will lit up.

Q20. A ring counter with 5 flip flops will have ……. states.

1. 5
2. 10
3. 32
4. Infinite

Answer : 1

Q21. For the gate in the given figure the output will be …….



1. 0
2. 1
3. A
4. $\bar{A}$

Answer : 4

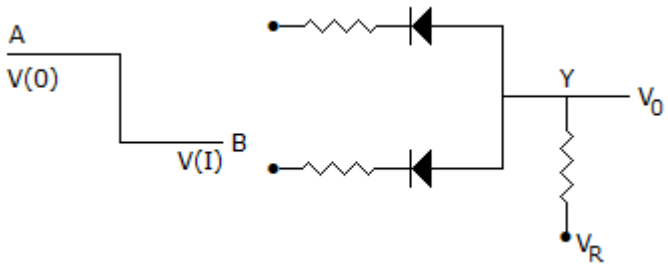
Explanation: If A = 0, Y = 1 and A = 1, Y = 0 Therefore Y = $\bar{A}$.

Q22. In the expression A + BC, the total number of minterms will be ……

1. 2
2. 3
3. 4
4. 5

Answer : 4

Q23. The circuit in the given figure is a …… gate.



1. positive logic OR gate
2. negative logic OR gate
3. negative logic AND gate
4. positive logic AND gate

Answer : 2

Explanation: Since V(1) is lower state than V(0) it is a negative logic circuit. Since diodes are in parallel, it is an OR gate.

Q24. Which of the following is non-saturating?

1. TTL
2. CMOS
3. ECL
4. Both 1 and 2

Answer : 3

Q25. The number of digits in octal system is ……

1. 8
2. 7
3. 9
4. 10

Answer : 1

Explanation: The octal system has 8 digits 0 to 7.

Q16.

Answer : 2

Explanation:

Q26. The access time of a word in 4 MB main memory is 100 ms. The access time of a word in a 32 kb data cache memory is 10 ns. The average data cache bit ratio is 0.95. The efficiency of memory access time is ……

1. 9.5 ns
2. 14.5 ns
3. 20 ns
4. 95 ns

Answer : 2

Explanation: Access time = 0.95 x 10 + 0.05 x 100.

Q27. The expression Y = pM (0, 1, 3, 4) is ……..

1. POS
2. SOP
3. Hybrid
4. none of these

Answer : 1

Explanation: This is a product of sums expression.

Q28. An 8 bit DAC has a full scale output of 2 mA and full scale error of ± 0.5%. If input is 10000000 the range of outputs is …….

1. 994 to 1014 μA
2. 990 to 1020 μA
3. 800 to 1200 μA
4. none of the above

Answer : 1

Explanation:

10000000 = 128, 11111111 = 255

If there is no error, output = $\frac{128}{255}$ x 2000 = 1004μA.

Maximum error = $\frac{2000 \times 0.5}{100}$ = ± 10 μA

Hence range of output 994 to 1014 μA.

Q29. Decimal 43 in hexadecimal and BCD number system is respectively……. and ……..

1. B2 and 01000011
2. 2B and 01000011
3. 2B and 00110100
4. B2 and 01000100

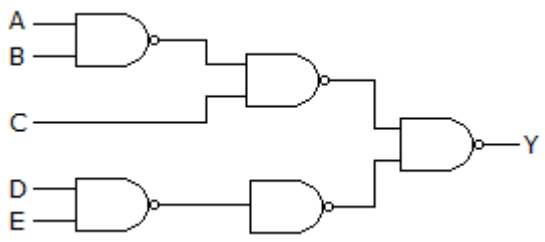
Answer : 2

Explanation:

$(43)_{10} = (2B)_{16}$

$(43)_{10} = (01000011)_2$.

Q30. The circuit of the given figure realizes the function ……



1. $Y = (\overline{A} + \overline{B})\, C + \overline{DE}$
2. $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$
3. AB + C +DE
4. AB + C(D + E)

Answer : 1

Explanation:

$Y = \overline{\overline{AB}C\ DE} = \overline{\overline{AB}\ C} + \overline{DE} = \overline{AB}\ C + \overline{DE}$ or

$Y = (\overline{A} + \overline{B})C + \overline{DE}.$

Q31. An AND gate has two inputs A and B and one inhibit input 3, Output is 1 if

1. A = 1, B = 1, S = 1
2. A = 1, B = 1, S = 0
3. A = 1, B = 0, S = 1
4. A = 1, B = 0, S = 0

Answer: 2

Explanation: All AND inputs must be 1 and inhibit 0 for output to be 1.

Q32. The greatest negative number which can be stored is 8 bit computer using 2's complement arithmetic is ……..

1. -256
2. -128
3. -255
4. -127

Answer: 2

Explanation: The largest negative number is 1000 0000 = -128.

Q33. A JK flip flop has t_{pd}= 12 ns. The largest modulus of a ripple counter using these flip flops and operating at 10 MHz is ……..

1. 16
2. 64
3. 128
4. 256

Answer: 4

Explanation:

$$\text{Number of flip-flops} = \frac{1}{12 \times 10^{-9} \times 10 \times 10^{6}} = \frac{1000}{120} = 8.333 \text{ say } 8$$

$$\text{Modulus} = 2^{8} = 256.$$

Q34. The basic storage element in a digital system is …….

1. flipflop
2. counter
3. multiplexer
4. encoder

Answer : 1

Explanation: Storing can be done only in memory and flip-flop is a memory element.

Q35. In a ripple counter,

1. whenever a flipflop sets to 1, the next higher FF toggles
2. whenever a flipflop sets to 0, the next higher FF remains unchanged
3. whenever a flipflop sets to 1, the next higher FF faces race condition
4. whenever a flipflop sets to 0, the next higher FF faces race condition

Answer : 1

Explanation: In a ripple counter the effect ripples through the counter.

Q36. A 12 bit ADC is used to convert analog voltage of 0 to 10 V into digital. The resolution is …….

1. 2.44 mV
2. 24.4 mV
3. 1.2 V
4. none of these

Answer : 1

Explanation:

$$\frac{10}{2^{12} - 1} \times 1000 = 2.44 \text{ mV}.$$

Q37. For the truth table of the given figure Y = ……..

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

1. A + B + C
2. $\bar{A}$ +BC
3. $\bar{A}$
4. B^{-}

Answer : 4

Explanation:

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + A\overline{B}\,\overline{C} + A\,\overline{B}\,C = \overline{A}\,\overline{B}\,(\overline{C} + C) + A\,\overline{B}\,(\overline{C} + C) = \overline{A}\,\overline{B} + A\overline{B} = \overline{B}(A + A) = \overline{B}.$$

Q38. A full adder can be made out of ……

1. two half adders
2. two half adders and a OR gate
3. two half adders and a NOT gate
4. three half adders

Answer : 2

Q39. If the functions *w, x, y, z* are as follows

$w = R + \overline{P}Q + \overline{R}S$,

$x = PQ\overline{R}\,\overline{S} + PQ\overline{R}\,\overline{S} + P\overline{Q}\,\overline{R}\,\overline{S}$

$y = RS + \overline{PR + P\overline{Q} + \overline{P}\overline{Q}}$

$z = R + S + \overline{PQ + \overline{P}\overline{Q} \cdot \overline{R} + P\overline{Q} \cdot \overline{S}}$

1. w = z x = z
2. w = z, x = y
3. w = y
4. w = y = z

Answer : 1

Q40. The output of a half adder is …….

1. Sum
2. Sum and Carry
3. Carry
4. none of these

Answer: 2

Q41. Minimum number of 2-input NAND gates required to implement the function F = (x + y) (Z + W) is ……..

1. 3
2. 4
3. 5
4. 6

Answer : 2

Explanation:

$F = (\bar{x} + \bar{y})\,(z + w) = \overline{xy}.(z + w)$

$= \overline{xy}z + \overline{xy}w$

$= \bar{\bar{F}} = \overline{\overline{\overline{xy}z + \overline{xy}\,w}} = \overline{\overline{\overline{xy}z} \,.\, \overline{\overline{xy}\,w}}$ minimum no. of 2 input NAND gate.

Q42. Which device has one input and many outputs?

1. Multiplexer
2. Demultiplexer
3. Counter
4. Flip flop

Answer: 2

Explanation: Demultiplexer takes data from one line and directs it to any of its N output depending on the status of its select lines.

Q43. A carry look ahead adder is frequently used for addition because

1. it costs less
2. it is faster
3. it is more accurate
4. uses fewer gates

Answer: 2

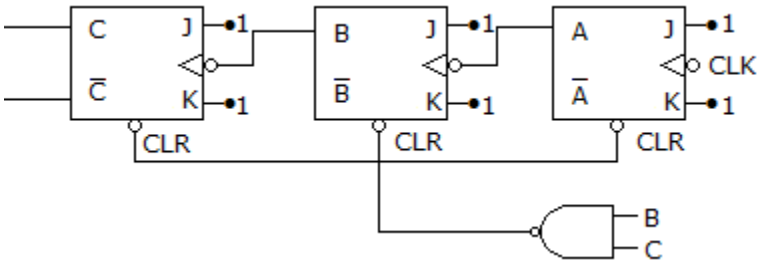
Explanation:

Q27.

Answer : 1

Explanation: In look ahead carry adder the carry is directly derived from the gates when original inputs are being added. Hence the addition is fast. This process requires more gates and is costly.

Q44. The counter in the given figure is …….



1. Mod 3
2. Mod 6
3. Mod 8
4. Mod 7

Answer : 2

Explanation: When counter is 110 the counter resets. Hence mod 6.

Q45. In register index addressing mode the effective address is given by ……..

1. index register value
2. sum of the index register value and the operand
3. operand
4. difference of the index register value and the operand

Answer : 2

Explanation:

4 = 2^2, in up scaling digit will be shifted by two bit in right direction.

Q46. $7BF_{16}$ = _____ $_2$

1. 0111 1011 1110
2. 0111 1011 1111
3. 0111 1011 0111
4. 0111 1011 0011

Answer : 2

Explanation:

$7BF_{16} = 7 \times 16^2 + 11 \times 16^1 + 15 \times 16^0 = 1983$ in decimal = 0111 1011 1111 in binary.

Q47. For the minterm designation Y = ∑ m (1, 3, 5, 7) the complete expression is ……..

1. $Y = \overline{A}\,\overline{B}C + A\,\overline{B}\,C$
2. $Y = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,C + ABC + \overline{A}\,BC$
3. $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}BC + A\,\overline{B}C$
4. $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}C + A\,\overline{B}C$

Answer : 2

Explanation:

Decimal number 1 = binary number 001 = $\overline{A}\,\overline{B}C$ Decimal number 7 = binary number 111= ABC, Decimal number 3 = binary number 011= $\overline{A}BC$ Decimal number 5 = binary number 101= $A\overline{B}C$. Hence result.

Q48. Zero suppression is not used in actual practice.

1. True
2. False

Answer: 2

Explanation: Zero suppression is commonly used.

Q49. A counter type A/D converter contains a 4 bit binary ladder and a counter driven by a 2 MHz clock. Then conversion time is ……..

1. 8 µ sec
2. 10 µ sec
3. 2 µ sec
4. 5 µ sec

Answer : 1

Explanation:

$$\text{Conversion time} = \frac{2^n}{\text{clock rate}} = \frac{2^4}{2 \times 10^6} = 8\ \mu\text{sec.}$$

$$\text{conversion rate} = \frac{1}{t_c} = \frac{1}{8 \times 10^{-6}} = 125 \text{ kilo conversions/sec.}$$

Q50. The hexadecimal number $(3E8)_{16}$ is equal to decimal number ……

1. 1000
2. 982
3. 768
4. 323

Answer : 1

Explanation: $3 \times 16^2 + 14 \times 16^1 + 8 = 1000$

Q51. The number of distinct Boolean expression of 4 variables is …….

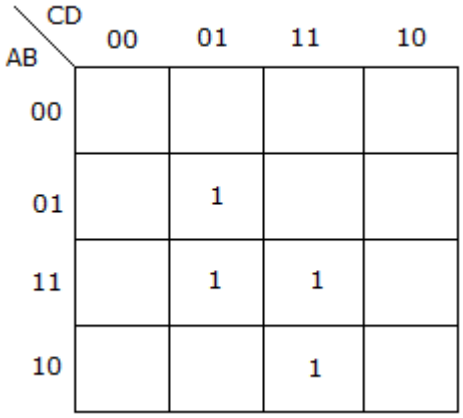
1. 16
2. 256
3. 1024
4. 65536

Answer : 4

Explanation:

$$2^{2^n} = 2^{2^4} = 2^{16}$$

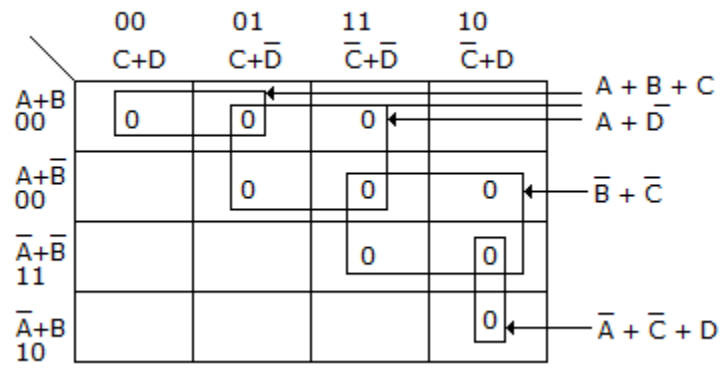
Q52. For the K map in the given figure the simplified Boolean expression is ……



1. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + ABC$
2. $\overline{A}\,C + \overline{A}\,\overline{D} + ABC$
3. $\overline{A}\,C + \overline{A}\,\overline{D} + ACD$
4. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + AB\,\overline{C}$

Answer : 1

Explanation:



Q53. A memory system of size 16 k bytes is to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is …….

1. 2
2. 4
3. 8
4. 18

Answer : 3

Explanation:

(16×1024×8)/(4096×4) = 8

Q54. In a 7 segment display, LEDs *b* and *c* lit up. The decimal number displayed is …….

1. 9
2. 7
3. 3
4. 1

Answer : 1

Q55. In a BCD to 7 segment decoder the minimum and maximum number of outputs active at any time is ….

1. 2 and 7
2. 3 and 7
3. 1 and 6
4. 3 and 6

Answer: 1

Explanation:

Minimum number of outputs when input is decimal 1 and maximum number of outputs when input is decimal 8.

Q56. A three state switch has three outputs. These are …….. , …….. , …….

1. low, low and high
2. low, high, high
3. low. floating, low
4. low, high, floating

Answer: 4

Q57. Maxterm designation for A + B + C is …….

1. M_0
2. M_1
3. M_3
4. M_4

Answer: 1

Explanation: A + B + C = 000 = M_0

Q58. 1's complement of 11100110 is …….

1. 00011001
2. 10000001
3. 00011010
4. 00000000

Answer: 1

Explanation: By replacing 1 by 0 and 0 by 1.

1. In the toggle mode a JK flip-flop has

A) J = 1, K = 0.
B) J = 0, K = 0.
C) J = 1, K = 1.
D) J = 0, K = 1.

2. A boolean function can be transformed into logical _____.

A) graph
B) diagram
C) map
D) matrix

3. A D-flip-flop is said to be transparent when

A) the output is HIGH
B) the output follows clock
C) the output follow input
D) the output is LOW

4. Which number system has a base of 16

A) Octal

B) Decimal
C) None
D) Hexadecimal

5. The boolean algebra is mostly based on

A) De Morgans theorem
B) De Morpans theorem
C) Standard theorem
D) Boolean theorem

6. If J = K (J and K are shorted) in a JK flip-flop, what circuit is made

A) K flip-flop
B) Shorted JK flip-flop
C) T flip-flop
D) SR flip-flop

7. In a T flip-flop no of input circuit is

A) 2
B) 4
C) 3
D) 1

8. A Binary number system has how many digits.

A) 1
B) 10
C) 0
D) 2

9. How many entries will be in the truth table of a 3 input NAND gate ?

A) 9
B) 6
C) 3
D) 8

10. In an SR latch built from NOR gates, which condition is not allowed

A) S=1, R=1
B) S=0, R=1
C) S=1, R=0
D) S=0, R=0

2. Truth table is used to express

A) Boolean matrix
B) Boolean expression
C) Boolean map
D) Boolean addition

3. OR operation is equivalant to

A) Both Union & Intersection
B) Union
C) Division
D) Intersection

4. The difference between the diagram of a NOR and OR gate is

A) OR has got a bubble at its output terminal
B) OR is more oval than NOR
C) NOR has got a bubble at its output terminal
D) OR is more squared than NOR

5. Latches are _____ circuits.

A) count triggered
B) pulse triggered
C) edge triggered
D) level triggered

6. AND operation is equivalant to

A) Division
B) Intersection
C) Union
D) Both Union & Intersection

7. The way of representing numbers in the form of 0s and 1s is called as

A) Ones Notation
B) Computer Notation
C) Binary Notation
D) Zeros Notation

8. Maximum number in decimal that can be represented by 4 bits (binary) is

A) 7
B) 4
C) 15
D) 16

9. Extended Binary Coded Decimal Interchange Code is an _____ bit code.

A) 32
B) 8
C) 16

D) 7

10. 2's Complement of 10101011 is

A) 00111100
B) 10101100
C) 01010101
D) 10101011

1. Convert hexadecimal value 16 to decimal.

   A. 22_{10}

   B. 16_{10}

   C. 10_{10}

   D. 20_{10}

   Answer: Option **A**

2. 2. Convert the following decimal number to 8-bit binary.
   187

   A. 10111011_2

   B. 11011101_2

   C. 10111101_2

   D. 10111100_2

   Answer: Option A

3. Convert binary 111111110010 to hexadecimal.

A. $EE2_{16}$

B. $FF2_{16}$

C. $2FE_{16}$

D. $FD2_{16}$

Answer: Option **B**

4. Convert the following binary number to decimal.
010112

A. 11

B. 35

C. 15

D. 10

Answer: Option A

5. Convert the binary number 1001.0010_2 to decimal.

A. 90.125

B. 9.125

C. 125

D. 12.5

Answer: Option **B**

6. Decode the following ASCII message.
`10100111010100101010110001001011001`
`01000001001000100000110100101000100`

A. STUDYHARD

7.

A. True

B. False

Answer: Option **B**

1. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

A. 1

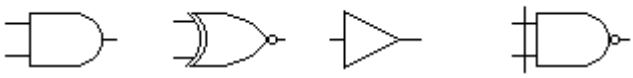
B. 2

C. 4

D. 8

Answer: Option **C**

2. Which of the figures shown below represents the exclusive-NOR gate?



a. b. c. d.

A. a

B. b

C. c

D. d

Answer: Option **B**

3.

A. 1111110

B. 1111101

C. 1111000

6.

A. 1111110

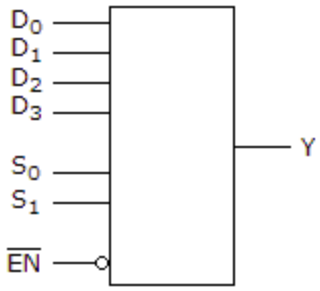
B. 1111101

C. 1111000

D. 1111111

Answer: Option **A**

4. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be LOW. What is the status of the Y output?



A. LOW

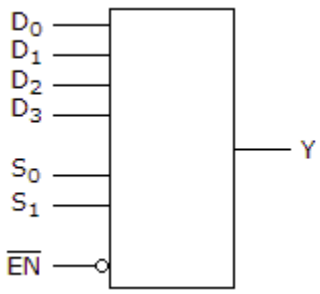
B. HIGH

C. Don't Care

D. Cannot be determined

Answer: Option **A**

5. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be HIGH. What is the status of the Y output?



A. LOW

B. HIGH

C. Don't Care

9. Which of the figures in figure (a to d) is equivalent to figure (e)?

A. a

B. b

C. c

D. d

Answer: Option **B**

14. The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal _____ gates with little or no increase in circuit complexity. (Select the response for the blank space that will BEST make the statement true.)

17. Which of the following combinations cannot be combined into K-map groups?

22.

A. $(A + B)(C + D)$

30. Looping on a K-map always results in the elimination of:

35.

2.

A. The logic level at the *D* input is transferred to *Q* on NGT of *CLK*.

B. The *Q* output is ALWAYS identical to the *CLK* input if the *D* input is HIGH.

C. The *Q* output is ALWAYS identical to the *D* input when *CLK* = PGT.

D. The *Q* output is ALWAYS identical to the *D* input.

- **A.** 1

- **B.** 4

- **C.** 6

6.

- **A.** 1

- **B.** 4

- **C.** 6

15.

A. The output toggles if one of the inputs is held HIGH.

B. Only one of the inputs can be HIGH at a time.

C. The output complement follows the input when enabled.

D. *Q* output follows the input *D* when the enable is HIGH.

Answer: Option **D**

22.

A. The output toggles if one of the inputs is held HIGH.

B. *Q* output follows the input *D* when the enable is HIGH.

C. Only one of the inputs can be HIGH at a time.

D. The output complement follows the input when enabled.

30.

A. the clock pulse is LOW

B. the clock pulse is HIGH

C. the clock pulse transitions from LOW to HIGH

C.

D.

Answer: Option **A**

53.

A. $J = 0, K = 0$

B. $J = 1, K = 0$

C. $J = 0, K = 1$

D. $J = 1, K = 1$

Answer: Option **A**

63.

66.

A. flip-flop is set

B. control input data has changed

C. flip-flop is reset

D. input data has no change

77.

A. No change will occur in the output.

B. An invalid state will exist.

C. The output will toggle.

D. The output will reset.

78.

A. 1 kHz

B. 2 kHz

C. 4 kHz

D. 16 kHz

Answer: Option **B**