F1900100 3021

3RD SEM./ ETC/ CSE/ IT/ AE&I/ EIC/Mechatronics / 2020(W)NEW

Th3- DIGITAL ELECTRONICS

Full Marks: 80 Time- 3 Hrs

Answer any five Questions including Q No.1& 2
Figures in the right hand margin indicates marks

1. Answer **All** questions 2 x 10
   a. State Demorgan's theorem.
   b. Why multiplexers are referred to as data selectors?
   c. Write down the necessity of A/D and D/A converters.
   d. What is universal shift registers?
   e. Define modulus of a counter.
   f. Define the term fan In and fan Out.
   g. Define racing condition in flip-flop. How it can be avoided?
   h. Convert (10110101) from binary to gray code.
   i. Perform 2's complement subtraction of 1000011-1010111.
   j. What is K-map?

2. Answer **Any Six** Questions 6 x 5
   a. Discuss 1:4 De-multiplexer with circuit, truth table and implementation by gates.
   b. Show the diagram of a clocked SR flip-flop. Explain its working with a functional table.
   c. Obtain the real minimal expression for f = $\sum m(1,2,4,6,7)$ and implement it using universal gates.
   d. Explain the working of SISO and PISO register with the help of suitable logic diagram.
   e. Simplify the Boolean expression: Y=AB+A(B+C)+B(B+C) and draw the logic circuit for the simplified function.
   f. Design an octal to binary encoder with neat circuit diagram.
   g. Write down all the characteristics of Digital ICs.

3. Show the logic diagram of clocked J-K flip-flop. Explain its working with a functional table with a neat circuit diagram. 10

4. Design a 3 bit magnitude comparator circuit for whose outputs are A>B, A<B and A=B where A & B are 3 bits binary numbers. 10

5. Which gates are referred to as Universal gates and why? How other gates can be implemented by using one of these gates? 10

6. Explain D/A conversion using R-2R ladder(weighted resistors) network. 10

7. Design a 2-bit asynchronous ripple counter (up and down) using flip-flop with a suitable logic diagram& timing diagram. 10