BRANCH- ELE SEMESTER- 4TH SUB:AE Lab		LESSON PLAN FACULTY NAME: NIHARIKA SETHY , LECT- ETC SEMESTER START: FROM: ___ / ___ / _____ TO ___ / ___ / _____ NO OF CLASSES ALLOTED PER WEEK-3	
WEEK		TOPICS TO BE COVERED	STATUS
W1		Determine the input and output Characteristics of CE & CB transistor configuration	
W2		Determine Drain & Transfer Characteristics of JFET	
W3		Construct Bridge Rectifier using different filter circuit and to determine Ripple factor & analyze wave form with filter & without filter.	
W4		Construct Bridge Rectifier using different filter and to determine Ripple factor.	
W5		Construct & test the regulator using Zener diode	
W6		Construct different types of biasing circuit and analyze the wave form (i) Fixed bias (ii) Emitter bias (iii) Voltage divider bias	
W7		Study the single stage CE amplifier & find Gain	
W8		Study multi stage R-C coupled amplifier & to determine frequency- response & gain.	
W9		Construct & Find the gain (I) Class A. Amplifier (ii) Class B. Amplifier (iii) Class C Tuned Amplifier	
W10		Construct & test push pull amplifier & observer the wave form	
W11		Construct & calculate the frequency of (i) Hartly Oscillator (ii) Collpit's Oscillator (iii) Wein Bridge Oscillator (iv) R-C phase shift oscillator and draw wave form & calculate the frequency	
W12		Construct & Test Differentiator and Integrator using R-C Circuit	
W13		Study Multivibrator (Astable, Bistable, Monstable) Circuit & Draw its Wave forms	
W14			
W15			
W16			

EXPERIMENT NO – 1

AIM OF THE EXPERIMENT:

To determine the input and output characteristics of CE and CB configuration.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS	SPECIFICATION	QUANTITY
1.	Transistor trainer kit		1No
2.	Single point patch cord	4 mm	As required
3.	DC Voltmeter	(0-1)V, (0-20)V	1 pc each
4.	DC Ammeter	(0-50)mA, (0-200 μA)	1 pc each
5.	Dual DC Power Supply pack	0-30 V	1 No.

THEORY:

A transistor is a three terminal active device. The terminals are emitter, base and collector. In a transistor, $I_E = I_B + I_C$

CE configuration: In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics are drawn between I_B and V_{BE} at constant V_{CE}. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and V_{CE} at constant I_B. The collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage.

Input Resistance = $\Delta V_{BE}/\Delta I_B$, Output resistance = $\Delta V_{CE}/\Delta I_C$

Current Amplification Factor (β)= $\Delta I_C/\Delta I_B$

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO} = \beta I_B + I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

This leakage current is represented by as I_{CEO}, i.e. collector-emitter current with base circuit is open.

CB configuration: In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased. The input characteristics are drawn between I_E and V_{BE} at constant V_{CB}. The output characteristics are drawn between Ic and V_{CB} at constant I_E.

Input Resistance = $\Delta V_{BE}/\Delta I_E$, Output resistance = $\Delta V_{CB}/\Delta I_C$

Current Amplification Factor (α)= $\Delta I_C/\Delta I_E$

$$I_C = \alpha I_E + I_{leakage} \quad \Longrightarrow \quad I_C = \alpha I_E + I_{CBO}$$

This leakage current is represented by as I_{CBO}, i.e. collector-base current with emitter circuit is open.

Comparision between CE, CB & CC configuration:-

S. No.	Characteristics	CB Configuration	CE Configuration	CC Configuration
1	Input resistance	Very low (40Ω)	Low (50Ω)	Very high (750kΩ)
2	Output resistance	Very high (1MΩ)	High (10kΩ)	Low (50Ω)
3	Current gain	Less than unity	High (100)	High (100)
4	Voltage gain	Small (150)	High (500)	Less than unity
5	Leakage current	Very small	Very large	Very large
6	Applications	For high frequency application	For audio frequency application	For impedance matching
7	Phase shift between input and output	0°	180°	0°

Circuit Diagram:

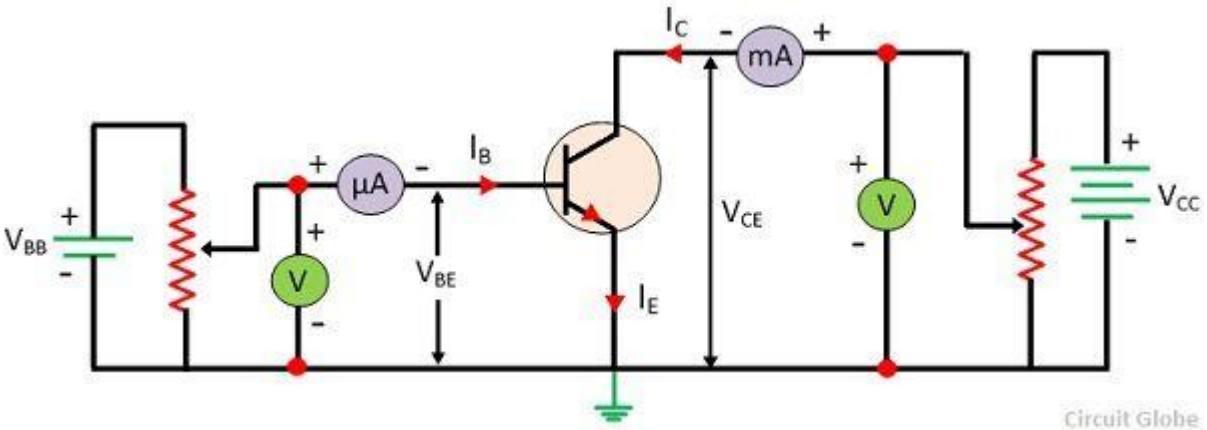


Fig. 1: CE configuration

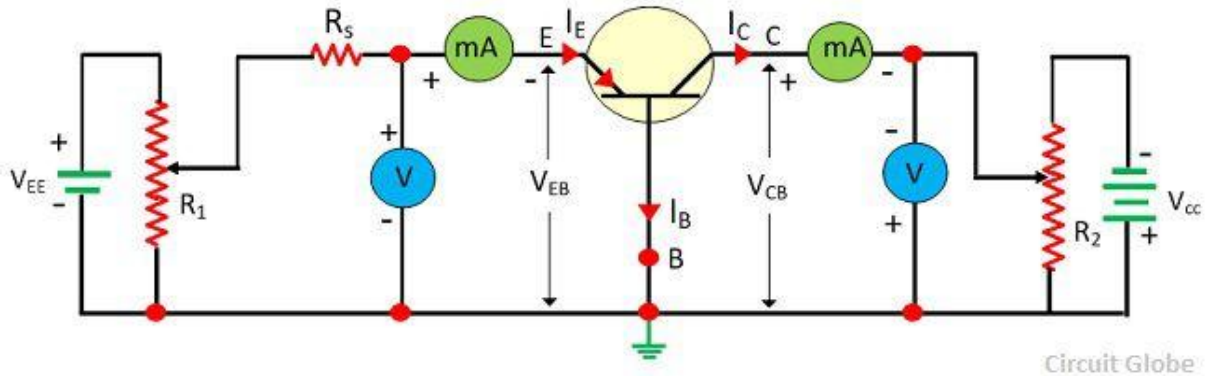


Fig. 2: CB configuration

PROCEDURE:

CE connection:

Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CE} constant at 2V and 6V.
3. Vary the I_B in steps and note down the corresponding V_{EB} values as per tabular column.

Output Characteristics:

1. Keep the I_B constant at 20 μA and 40 μA.
2. Vary the V_{CE} in steps and note corresponding I_C values.
3. Readings are tabulated as shown in tabular column.

CB Characteristics:

Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CB} constant at 0V and 10V.
3. Vary the I_E in steps and note down the corresponding V_{EB} values as per tabular column.

Output Characteristics:

1. Keep the I_E constant at 0.5 mA and 2 mA.
2. Vary the V_{CB} in steps and note corresponding I_C values.
3. Readings are tabulated as shown in tabular column.

OBSERVATION:

CE Connection:

Input Characteristic

V_{CE} = 2V		V_{CE} = 6V	
V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)

Output Characteristic

I_B = 20 μA		I_B = 40 μA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

CB Connection:

Input Characteristic

V_{CB} = 0V		V_{CB} = 10V	
V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)

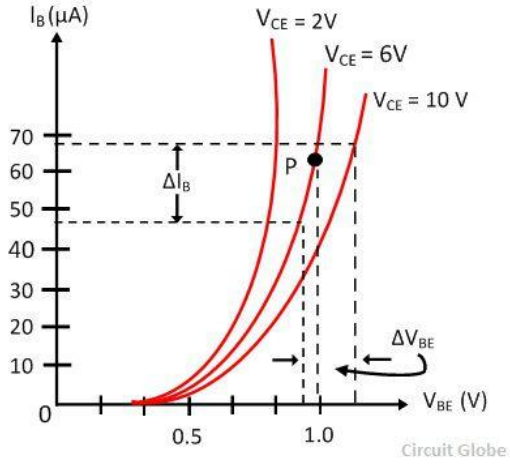
Output Characteristic

I_E = 0.5 mA		I_E = 2 mA	
V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)

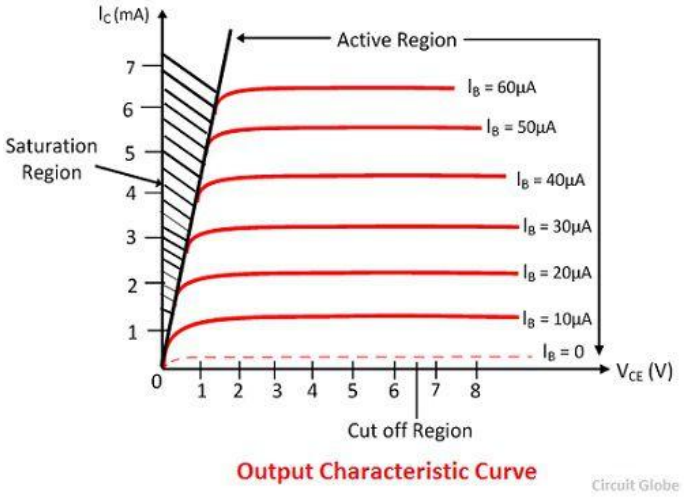
Graph:

Plot the input and output characteristics curve of CE and CB configuration from the data obtained in the graph paper. The expected graphs are shown below:

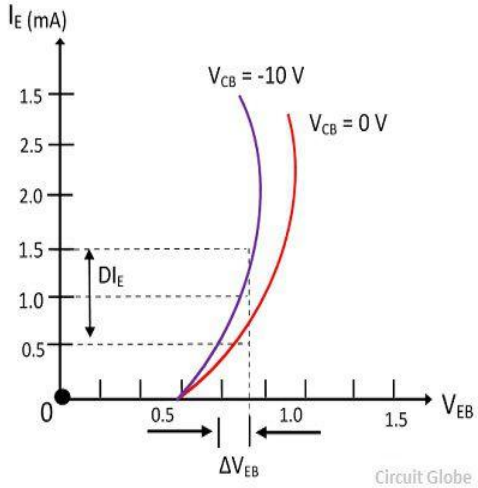
CE connection-



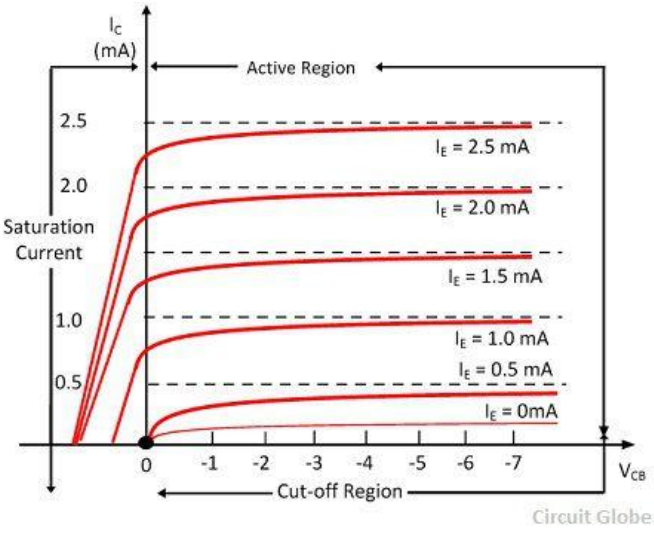
(Input Characteristics curve)



CB connection-



(Input Characteristics curve)



(Output Characteristics curve)

PRECAUTIONS:

1. Keep the knobs of supply voltages V_{BE} & V_{CE} at minimum positions when switching ON or switching OFF the power supply.
2. While performing the experiment do not exceed the ratings of the BJT. This may lead to damage the BJT.
3. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
4. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
5. Make sure while selecting the emitter, base and collector terminals of the transistor.

CONCLUSION:

1. Input and output characteristics of CE and CB configured transistor are studied.
2. Input resistance, output resistance and current amplification factor can also be measured.

EXPERIMENT NO – 2

AIM OF THE EXPERIMENT:

To determine the drain and transfer characteristics of FET.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS	SPECIFICATION	QUANTITY
1.	FET trainer kit	ME-535	1No
2.	Single point patch cord	4 mm	9 Nos

THEORY:

A field effect transistor is a three terminal semi-conductor device in which current conduction is by one type of carrier i.e electrons or holes. It is a unipolar device. The field effect transistor is fabricated by using monolithic silicon technology. It has 3 terminals: Gate, Source and Drain. A JFET can be used in any of the three configurations viz, Common Source, Common Gate and Common Drain. The input gate to source junction should always be operated in reverse bias, hence input resistance $R_i = \infty$, $I_G \approx 0$. FET is a voltage controlled constant current device in which variable input voltage controls the output current.

Pinch off voltage Vp is defined as the gate to source reverse bias voltage at which the output drain current becomes zero. In CS configuration Gate is used as input node and Drain as the output node. A JFET in CS configuration is used widely as an amplifier. A JFET amplifier is preferred over a BJT amplifier when the demand is for smaller gain, high input resistance and low output resistance.
The drain current equation in the active region is given as

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Where I_{DSS} is called as Drain to Source Saturation current & Vp is called as the Pinch off voltage.

There are two types of static characteristics of JFET viz
(1) Output or drain characteristic and
(2) Transfer characteristic.

The curve drawn between drain current I_D and drain-source voltage V_{DS} with gate-to source voltage V_{GS} as the parameter is called the *drain* or *output characteristic.* This characteristic is analogous to collector characteristic of a BJT.

The curve drawn between gate-source voltage V_{GS} and drain current I_D at constant drain-source voltage V_{DS} is called the *transfer characteristics*. This characteristic is analogous to transconductance characteristic of a BJT.

Circuit Diagram:

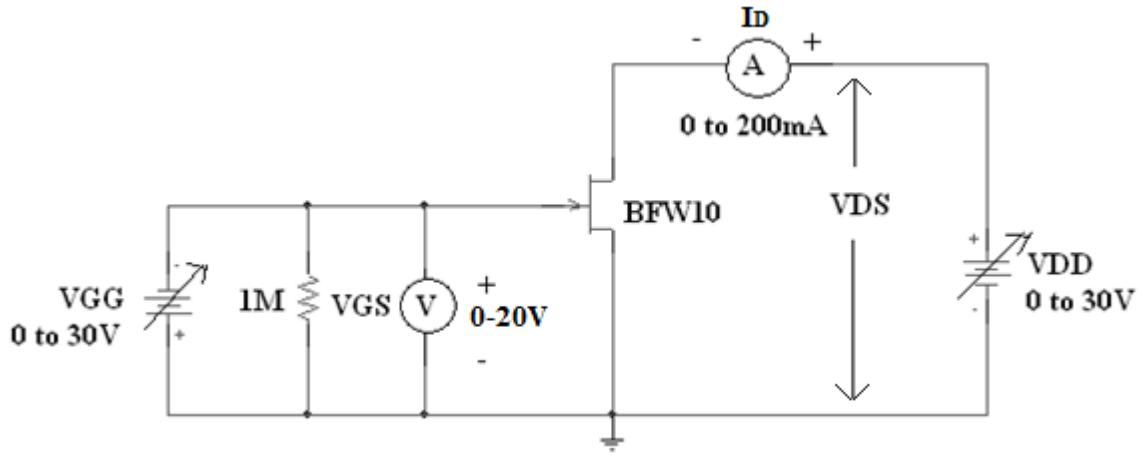


Fig. 1: Characteristics of FET

PROCEDURE:

Transfer Characteristics:

1) Connect the circuit as shown in figure. All the knobs of the power supply must be at the minimum position before the supply is switched on.
2) Adjust the output voltage V_{DS} to 4V by adjusting the supply V_{DD}.
3) Vary the supply voltage V_{GG} so that the voltage V_{GS} varies in steps of -0.25 V from 0 V onwards. In each step note the drain current I_D. This should be continued till I_D becomes zero.
4) Repeat above step for V_{DS} = 8 V.
5) Plot a graph between the input voltage V_{GS} and output current I_D for output voltage V_{DS} in the second quadrant. This curve is called the transfer characteristics.

Drain Characteristics:

1) Connect the circuit as shown in figure. Adjust all the knobs of the power supply to their minimum positions before switching the supply on.
2) Adjust the input voltage V_{GS} to 0 V by adjusting the supply V_{GG}.
3) Vary the supply voltage V_{DD} so that V_{DS} varies in steps of 0.5 V from 0 to 4 V and then in steps of 1 V from 4 to 10 V. In each step note the value of drain current I_D.
4) Adjust V_{GS} to -1 and -2 V and repeat step-3 for each value of V_{GS}.
5) Plot a graph between V_{DS} and I_D for different values of V_{GS}. These curves are called drain characteristics.
6) Mark the various regions in the drain characteristics graph and calculate the drain resistance.

OBSERVATION:

TRANSFER CHARACTERISTICS:

Sl	Vds = 4V		Vds = 8V	
1	Vgs (V)	Id (mA)	Vgs (V)	Id (mA)
2				
3				
4				
5				
6				

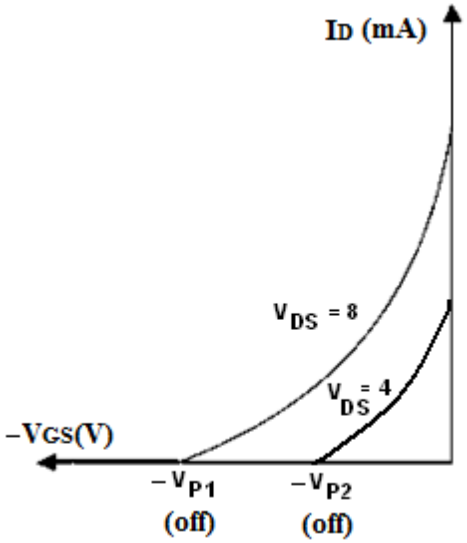
DRAIN CHARACTERISTICS:

Sl	Vgs = 0V		Vgs = -1V		Vgs = -2V	
1	Vds (V)	Id (mA)	Vds (V)	Id (mA)	Vds (V)	Id (mA)
2						
3						
4						
5						
6						

Graph:

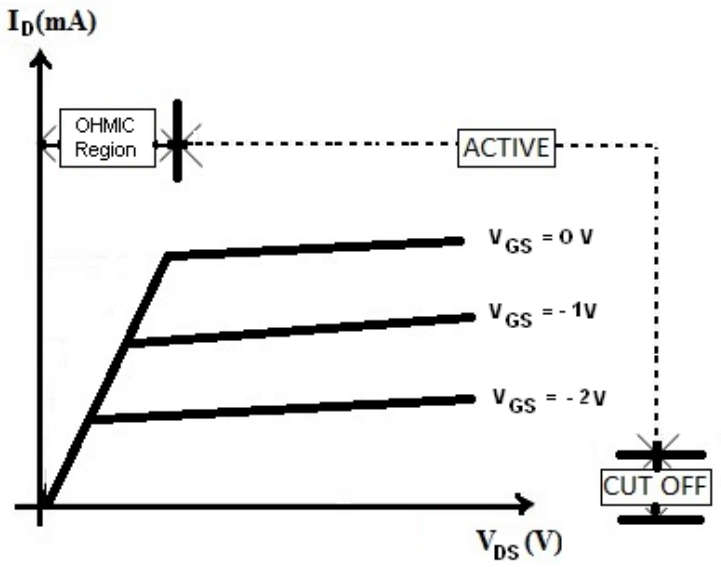
Transfer Characteristics -

1. Plot the transfer characteristics by taking V_{GS} on X-axis and taking I_D on Y-axis at constant V_{DS}.



Drain Characteristics -

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at a constant V_{GS}.



PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the transistor.

RESULTS:

1. Drain Characteristics and Transfer Characteristics of a Field Effect (FET) Transistor are studied.
2. Drain resistance, trans-conductance and amplification factor can also be measured.

EXPERIMENT NO – 3

AIM OF THE EXPERIMENT:

Construct a bridge rectifier using different filter circuit and to determine ripple factor and analyze waveform with filter and without filter.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS/COMPONENTS	SPECIFICATION	QUANTITY
1.	Diode	1N4007	4 no
2.	Transformer -step down	220V/9V, 50Hz	1 no
3.	Decade Resistance box	10Ω -100 KΩ	1 no
4.	Capacitor	100 µF	2 no
5.	Inductor	35 mH	1 no
6.	CRO	(0-20) MHz	1 pc
7.	CRO Probes		2 pair
8.	Ammeter	0-200µA/200mA	1 pc
9.	DC/AC Voltmeter	(0-20) V	1 pc each
10.	Connecting wires		

THEORY:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components. A full wave rectifier makes use of either two or four diodes to carry out this conversion. It is named so as the conversion occurs for complete input signal cycle. The full-wave bridge rectifier consists of four diodes connected in bridge fashion. During the positive half cycle, a positive voltage appears at the anode of D1 & D3 while a negative voltage appears at the anode of D2 & D4. Due to this diode D1 & D3 are forward biased it results in a current Id1 through the load R. During the negative half cycle, a positive voltage appears at the anode of D2 & D4 and hence it is forward biased. Resulting in a current Id2 through the load at the same instant a negative voltage appears at the anode of D1 & D3 thus reverse biasing it and hence it doesn't conduct.

Ripple Factor: Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol 'γ'. $\gamma_{FWR} = VAC/VDC = 0.48$

Rectification Factor: The ratio of output DC power to input AC power is defined as efficiency. It is denoted by 'η'. $\eta = (VDC)^2/(VAC)^2 = 81.2\%$

In DC supplies, a rectifier is often followed by a filter circuit which converts the pulsating DC signal into pure DC signal by removing the AC component or ripple. A **capacitor-input filter** or shunt capacitor filter is a filter circuit in which the first element is a capacitor connected in parallel with the output of the rectifier in a linear power supply. An L-section filter consists of an inductor and a capacitor connected in the form of an inverted L which is called **choke input filter**. A π- section filter consists of two capacitors and one inductor in the form symbol pi which is called **Capacitor filter**.

In filter circuit, Inductor offers a low reactance to DC component of rectifier output; therefore it blocks AC but passes DC at the output. Capacitor offers a low reactance to AC component of rectifier output which could not be blocked by an inductor 'L' and only the DC component is available at the output. Capacitor blocks DC but passes AC.

Circuit Diagram:

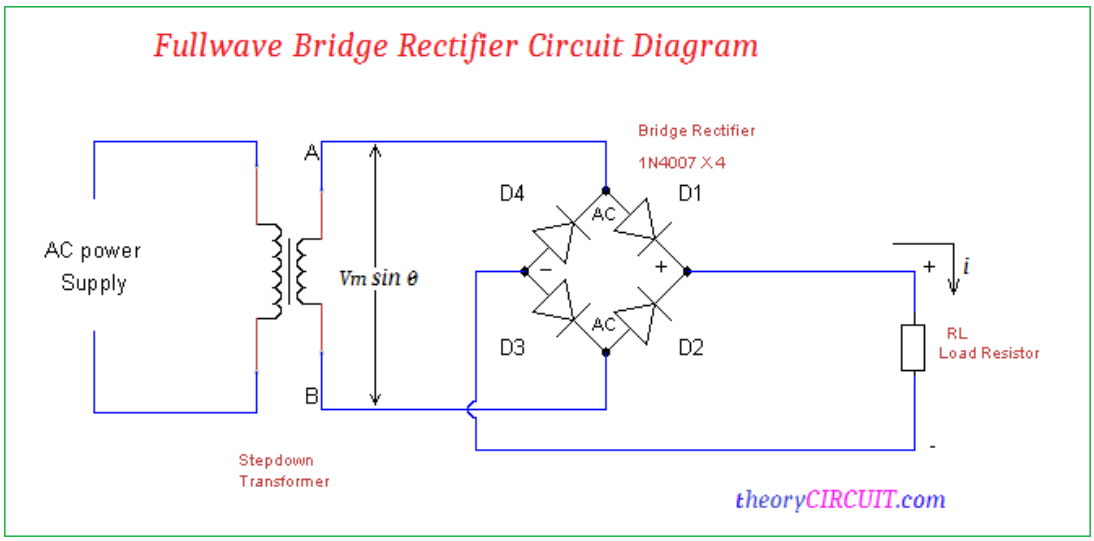
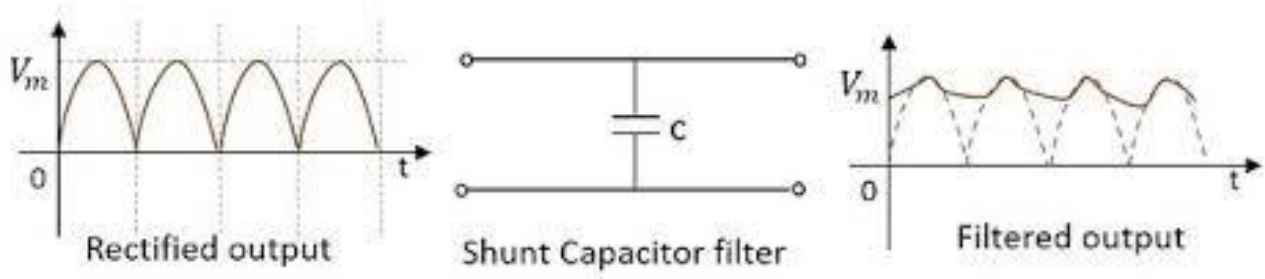
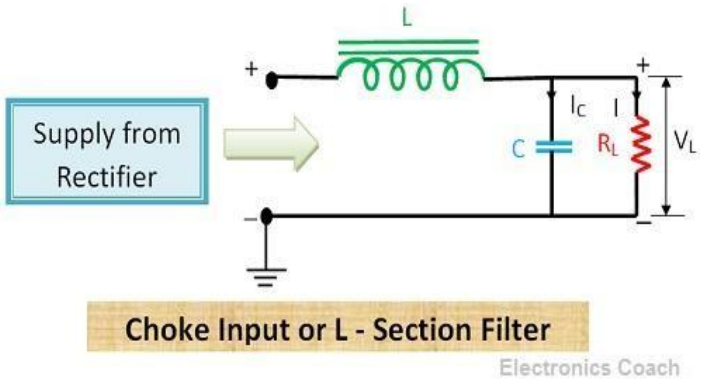


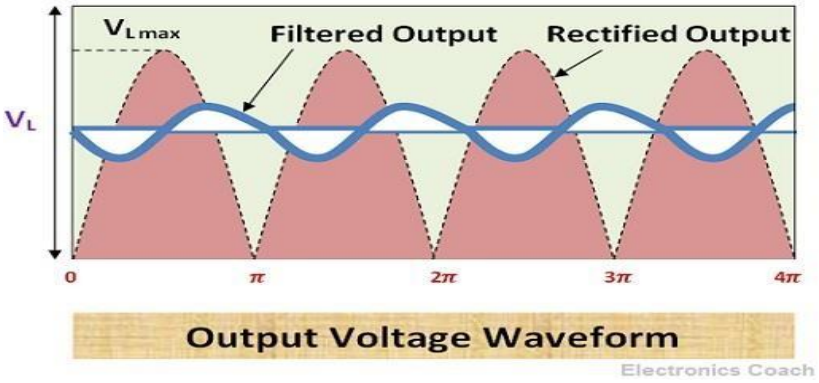
Fig. 1: Bridge rectifier without filter

Shunt capacitor filter:-

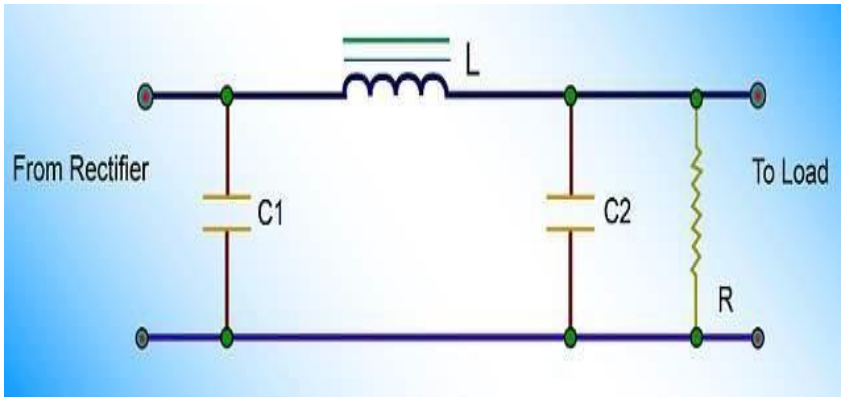


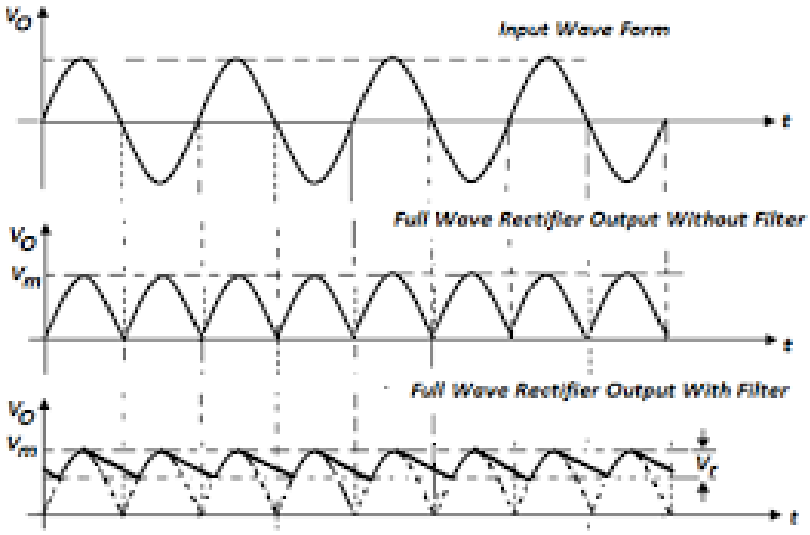
Choke input filter:-





Pi filter:-





PROCEDURE:

Full-wave Bridge Rectifier without filter -

1. Connect the circuit as shown in the figure 1.
2. Adjust the load resistance RL to 500 ohm and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance RL and repeat the procedure as the above.
5. Readings are to tabulate as per the tabular column.

Full-wave Rectifier with filter -

1. Connect the rectifier circuit output to different filter circuit as shown in the figure.
2. Adjust the load resistance RL to 500 ohm and connect the filter circuit in parallel with the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance RL and repeat the procedure as the above.
5. Readings are to tabulate as per the tabular column.

OBSERVATION:

Full-wave Bridge Rectifier without filter-

Load Resistance (RL)	Input Signal		Output Signal		Idc (mA)	VAC(V)	VDC(V)	Ripple factor=γ_{FWR} =VAC/VDC
	Vm p-p(v)	Freq (Hz)	Vm p-p(v)	Freq (Hz)				
500Ω								
1KΩ								
2KΩ								
10KΩ								

Full-wave Bridge Rectifier with filter -

Load Resistance (RL)	Input Signal		Output Signal		Idc (mA)	VAC(V)	VDC(V)	Ripple factor=γ_{FWR} =VAC/VDC
	Vm p-p(v)	Freq (Hz)	Vm p-p(v)	Freq (Hz)				
500Ω								
1KΩ								
2KΩ								
10KΩ								

PRECAUTIONS:

1. While performing the experiment do not exceed the voltage ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities to measure Vdc, Vac & Idc.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULTS:

Ripple factor of full wave bridge rectifier without filter is =
Ripple factor of full wave bridge rectifier with filter is =

Hence, it is concluded that capacitor or Pi filter is the best filter circuit and the output of rectifier followed by capacitor or Pi filter is pure DC. More pure dc o/p can be obtained by using multistage and appropriate filter circuit

EXPERIMENT NO – 4

AIM OF THE EXPERIMENT:

Construct a Centre tapped full wave rectifier using different filter circuit and to determine ripple factor and analyze waveform with filter and without filter.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS/COMPONENTS	SPECIFICATION	QUANTITY
1.	Diode	1N4007	2 no
2.	Transformer -step down	220V/9V, 50Hz	1 no
3.	Decade Resistance box	10Ω -100 KΩ	1 no
4.	Capacitor	100 µF	2 no
5.	Inductor	35 mH	1 no
6.	CRO	(0-20) MHz	1 pc
7.	CRO Probes		2 pair
8.	Ammeter	0-200µA/200mA	1 pc
9.	DC/AC Voltmeter	(0-20) V	1 pc each
10.	Connecting wires		

THEORY:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components. A full wave rectifier makes use of either two or four diodes to carry out this conversion. It is named so as the conversion occurs for complete input signal cycle. The full-wave centre tapped rectifier consists of two diodes and a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased it results in a current Id1 through the load R. During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased. Resulting in a current Id2 through the load at the same instant a negative voltage appears at the anode of D1, thus reverse biasing it and hence it doesn't conduct.

Ripple Factor: Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol 'γ'. $\gamma_{FWR} = VAC/VDC = 0.48$

Rectification Factor: The ratio of output DC power to input AC power is defined as efficiency. It is denoted by 'η'. $\eta = (VDC)^2/(VAC)^2 = 81.2\%$

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In filter circuit, Inductor offers a low reactance to DC component of rectifier output; therefore it blocks AC but passes DC at the output. Capacitor offers a low reactance to AC component of

rectifier output which could not be blocked by an inductor 'L' and only the DC component is available at the output. Capacitor blocks DC but passes AC.

Circuit Diagram:

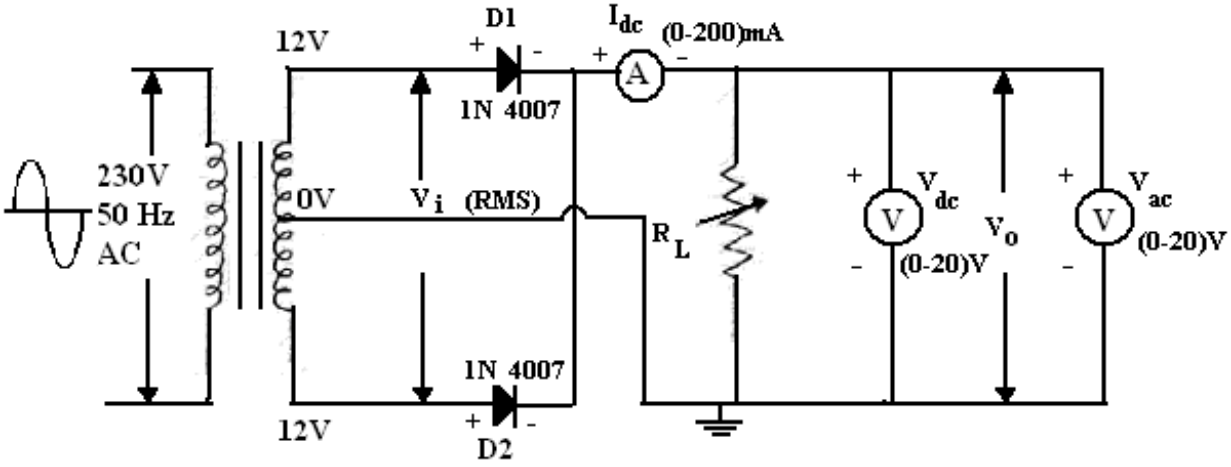


Fig. 1: Centre tapped rectifier without filter

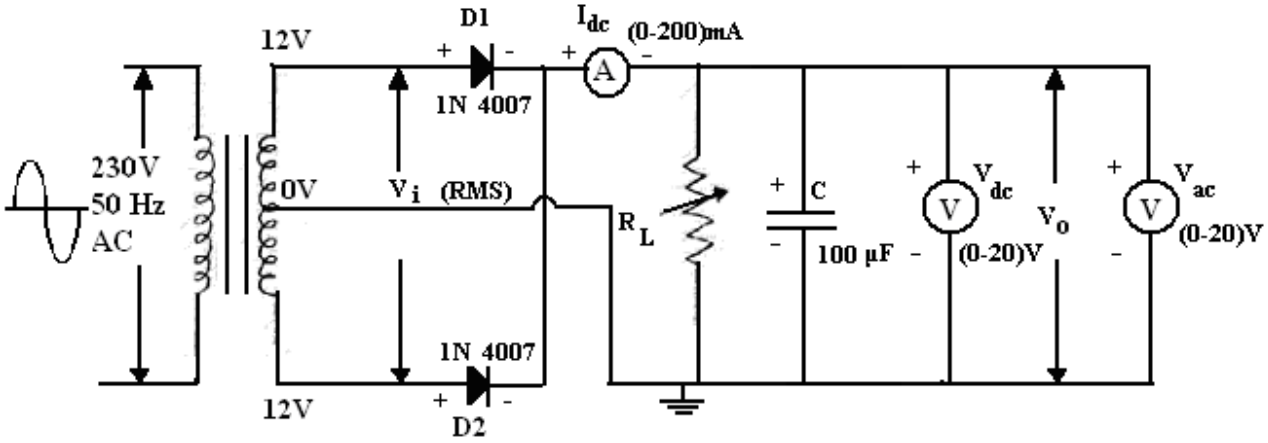
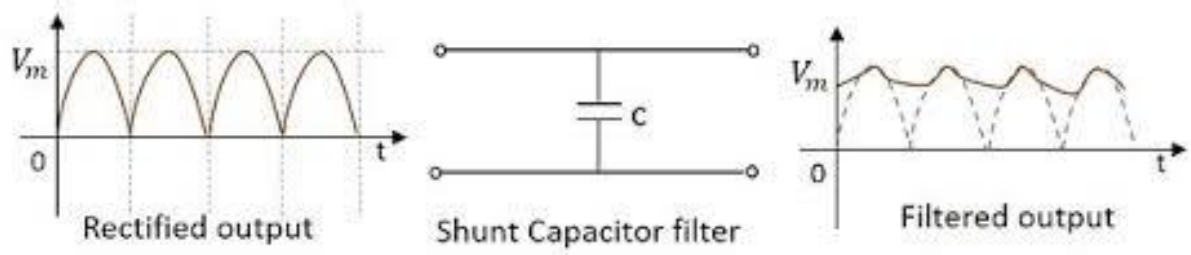
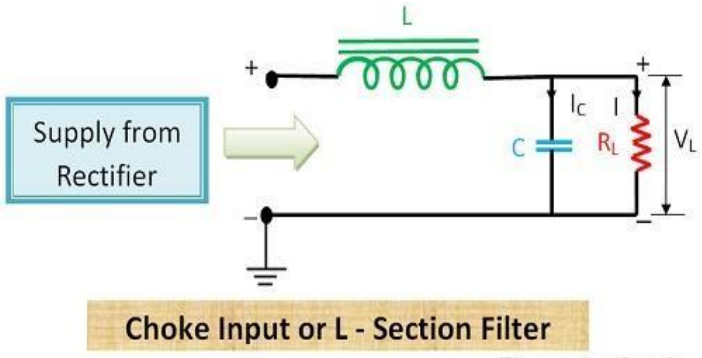


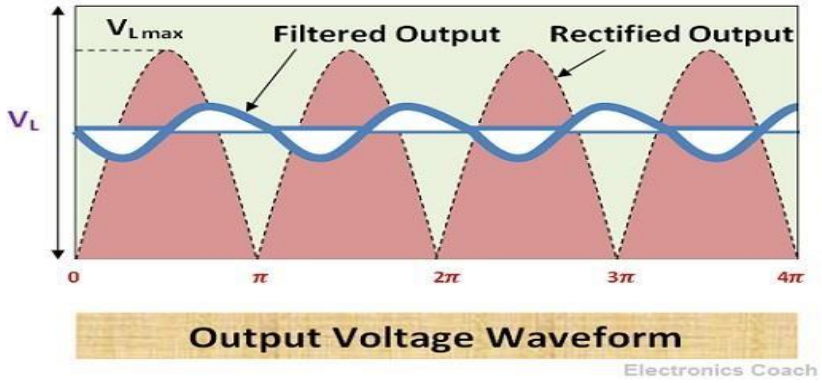
Fig. 2: Centre tapped rectifier with filter

Shunt capacitor filter:-

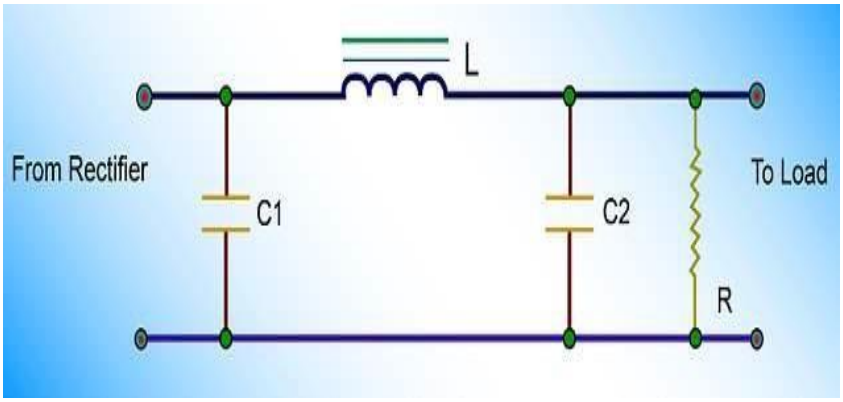


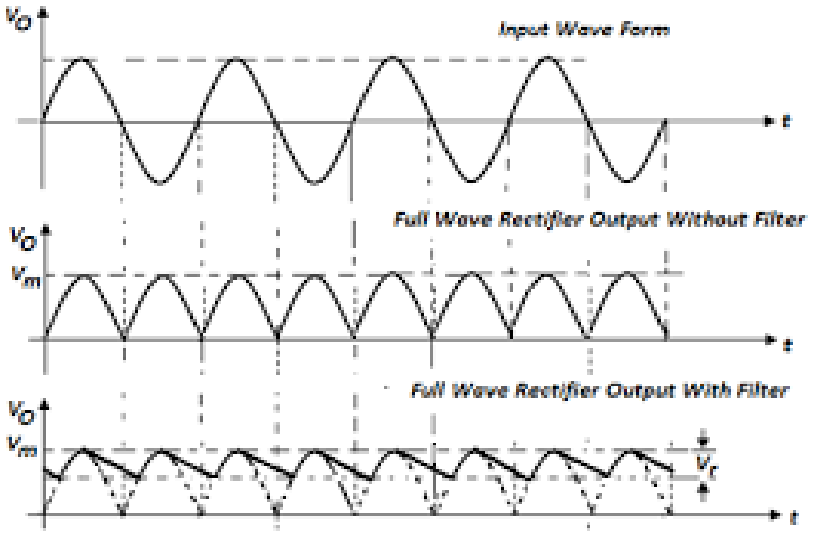
Choke input filter:-





Pi filter:-





PROCEDURE:

Full-wave Centre tap Rectifier without filter -

1. Connect the circuit as shown in the figure 1.
2. Adjust the load resistance RL to 500 ohm and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance RL and repeat the procedure as the above.
5. Readings are to tabulate as per the tabular column.

Full-wave Centre tap Rectifier with filter -

1. Connect the rectifier circuit output to different filter circuit as shown in the figure.
2. Adjust the load resistance RL to 1K ohm and connect the filter circuit in parallel with the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance RL and repeat the procedure as the above.
5. Readings are to tabulate as per the tabular column.

OBSERVATION:

Full-wave Centre tapped Rectifier without filter-

Load Resistance (RL)	Input Signal		Output Signal		Idc (mA)	VAC(V)	VDC(V)	Ripple factor=γ_{FWR} =VAC/VDC
	Vm p-p(v)	Freq (Hz)	Vm p-p(v)	Freq (Hz)				
500Ω								
1KΩ								
2KΩ								
10KΩ								

Full-wave Centre tapped Rectifier with filter -

Load Resistance (RL)	Input Signal		Output Signal		Idc (mA)	VAC(V)	VDC(V)	Ripple factor=γ_{FWR} =VAC/VDC
	Vm p-p(v)	Freq (Hz)	Vm p-p(v)	Freq (Hz)				
500Ω								
1KΩ								
2KΩ								
10KΩ								

PRECAUTIONS:

1. While performing the experiment do not exceed the voltage ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities to measure Vdc, Vac & Idc.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULTS:

Ripple factor of full wave centre tapped rectifier without filter is =
Ripple factor of full wave centre tapped rectifier with filter is =

Hence, it is concluded that capacitor or Pi filter is the best filter circuit and the output of rectifier followed by capacitor or Pi filter is pure DC. More pure dc o/p can be obtained by using multistage and appropriate filter circuit

EXPERIMENT NO – 5

AIM OF THE EXPERIMENT:

Construct and test the voltage regulator using Zener Diode.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Resistance	1kohm, 0.5w	1 No
2.	Variable Resistance	0-20 Kohm	1 No
3.	Zener Diode	4.7V (1N4735A)	1 No
4.	DC Variable Power Supply	0-15 V	1 No
5.	Digital/Analog Multimeter		1 No
6.	Digital Ammeter	0-200mA	1 No
7.	Digital Voltmeter	0-20 V	1 No
8.	Connecting Wire		As Per Required

THEORY:

Zener diode is a heavily doped Silicon diode. An ideal P-N junction diode does not conduct in reverse biased condition. A Zener diode conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage. A Zener diode when forward biased behaves like an ordinary P-N junction diode and when reverse biased acts as a voltage regulator. A Zener diode when reverse biased can undergo avalanche break down or zener break down.

Avalanche Break down:

If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction increases the kinetic energy of the charge carriers which collides with the adjacent atoms and generates charge carriers by breaking the bond, they in-turn collides with other atoms by creating new charge carriers, this process is cumulative which results in the generation of large current resulting in **Avalanche** Breakdown.

Zener Break down:

The basic principle of zener diode is the zener break down. If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces, it leads to the development of strong electric field and application of even a small voltage at the junction may rupture covalent bond and generate large number of charge carriers. Such sudden increase in the number of charge carriers results in **Zener** break down.

- under all conditions , Vin = IR+Vz = IR + Vout
- Vout = Vz, where Vz is called zener breakdown voltage

Load regulation =(voltage at no load –voltage at full load)/voltage at no load

Line regulation =change in output/change in input voltage.

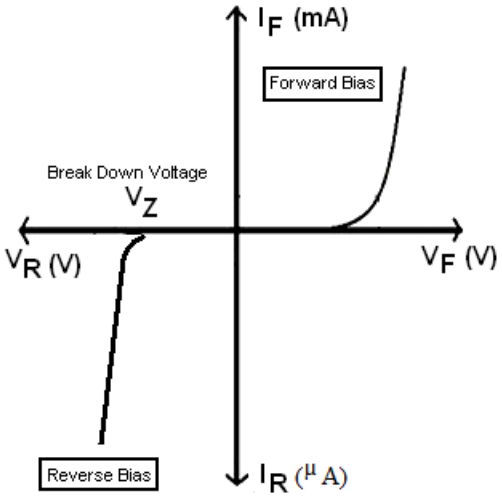


Fig 1: V-I characterstics of Zener diode

Circuit Diagram:

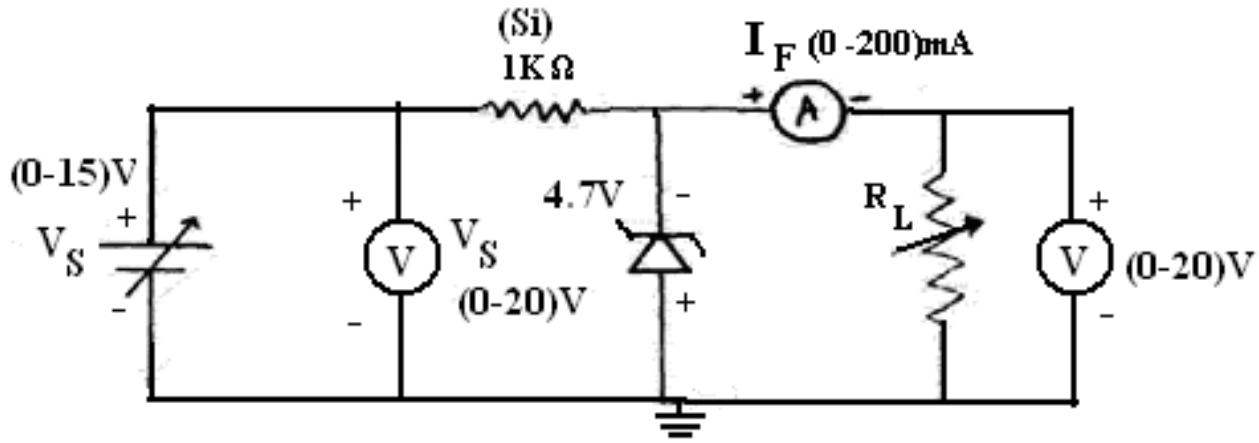


Fig. 2: Zener diode Voltage regulator

PROCEDURE:

Reverse Bias Condition:

1. Connect the Zener diode in reverse bias as shown in the fig.2.
2. Vary the voltage across the diode in step of 1V from 0 to 2V and then steps of 2 V from 2 V to 14 V. In each step, note down the current flowing through the diode and output voltage i.e. voltage across the zener diode.

OBSERVATION:

Zener Diode As Voltage Regulator:
Vin=15V , VNL =____

RL(Ω)	V_{FL} (volts)	I_L (mA)	%Regulation
100			

200			
500			
1K			
2K			
5K			
10K			
20K			

RL=15K

Es (volts)	E_{FL} (volts)	I_L (mA)
1		
2		
4		
6		
8		
10		
12		
14		

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the zener diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULTS:

1. The Zener Diode Characteristics have been studied.
2. The breakdown voltage of Zener diode in reverse bias was found to be = _____

EXPERIMENT NO – 6

AIM OF THE EXPERIMENT:

Construct different types of biasing circuit and analyze the wave form of the

(a) Fixed Bias (b) Emitter Bias (C) Voltage divider Bias

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Transistor biasing kit		1 No
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

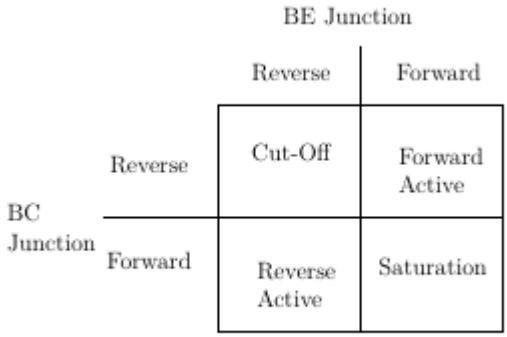
THEORY:

Transistor biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. It is required to activate the transistor and prevents it to either to saturation mode or cut-off mode. A bipolar transistor is biased so that the Q-point is near the middle of its operating range, which is approximately halfway between cut-off and saturation. This allows the output voltage to increase and decrease around the amplifiers Q-point without distortion as the input signal swings through one complete cycle. The different biasing methods used in bipolar transistor amplifiers are:

(i) Fixed bias or base resistor method or fixed base bias.
(ii) Collector-to-base bias or Collector feedback bias.
(iii) Dual Feedback bias
(iv) Fixed bias with emitter resistor.
(v) Emitter bias
(vi) Emitter feedback bias
(vii) Voltage divider bias or potential divider

Fixed bias is when the biasing circuit is independent of changes in transistor parameters and is solely dependent on supply and biasing circuit made up of passive components. Self bias is when some parameter of transistorized circuit (voltage/current) is connected to the biasing circuit, such that the changes in transistor parameter affect its own biasing circuit.

Depending on the bias of each of the two p-n junctions, the BJT operates in one of four distinct regions:



In linear applications, BJT circuits must be designed so that the transistor operates in the forward-active region. In order to insure operation in the forward-active region, the transistor is biased at a quiescent operating point, commonly called the Q-point, based on the DC conditions of the BJT. The quiescent point is determined by the transistor input and output characteristics and the applied currents and voltages. The quiescent point is defined by the BJT DC quantities VBE, IB, VCE, and IC. These points may be determined through the use of load-line analysis and design methods.

Fixed Base Biasing

The circuit of Fixed bias is shown in fig 1. In this method, the transistors base current, I_B remains constant for given values of Vcc, and therefore the transistors operating point must also remain fixed. This two resistor biasing network is used to establish the initial operating region of the transistor using a fixed current bias.

Emitter Biasing

The circuit of Emitter bias is shown in fig 2. Emitter bias method provides the best stability with respect to the β variation or temperature. This biasing network uses two supply voltages, V_{CC} and V_{EE} , which are equal but opposite in polarity. Here VEE forward biases the Base-Emitter junction using RE while VCC reverse biases the collector-Emitter junction. In this kind of biasing, I_C can be made independent of both β and V_{BE} by choosing $R_E >> R_B/\beta$ and $V_{EE} >> V_{BE}$, respectively; which results in a stable operating point.

Voltage Divider Biasing

The circuit of voltage divider or self bias is shown in fig 3. Here the common emitter transistor configuration is biased using a voltage divider network to increase stability. Resistors R_{B1} and R_{B2} form a voltage or potential divider network across the supply. This voltage divider biasing configuration is the most widely used transistor biasing method. The emitter diode of the transistor is forward biased by the voltage value developed across resistor R_{B2}. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the biasing voltages set at the transistors base, emitter, and collector terminals are not dependant on external circuit values.

Stability Factor (S): It is defined as the rate of change of collector current IC with respect to the collector base leakage current ICO, keeping both the current IB and the current gain β constant.

$$S=\partial IC/\partial ICO=dIC/dICO=\Delta IC/\Delta ICO$$

In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible.

For fixed bias, stability factor reduces to $S = 1 + \beta$

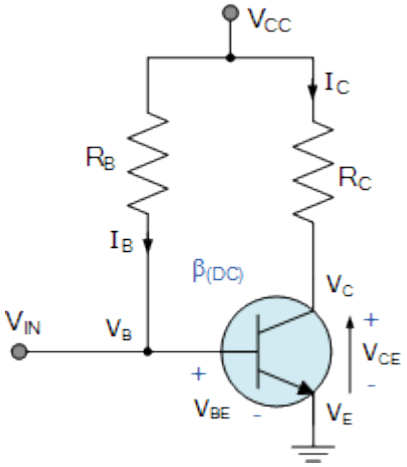
Since β is large quantity, this is a very poor bias stable circuit.

For emitter bias, stability factor (S) $=(1+\beta)*(RB+RE)/\{RB+(1+\beta)RE\}$

As can be seen, this value of the stability factor is smaller than the value obtained by fixed bias circuit.

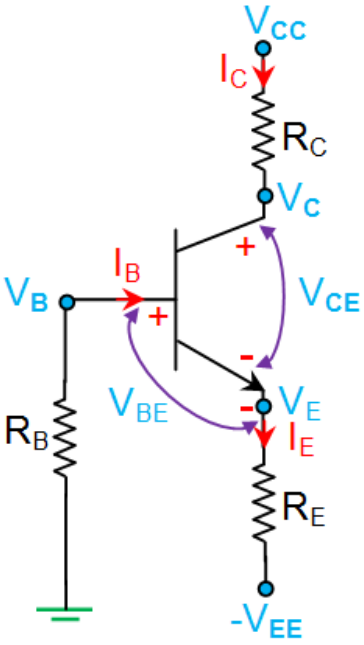
For self-bias, stability factor (S) =(1+β)*(1+RB/RE)/(1+β+RB/RE) where RB = (RB1*RB2)/(RB1+RB2). Ideally for self bias, S=1.

Circuit Diagram:



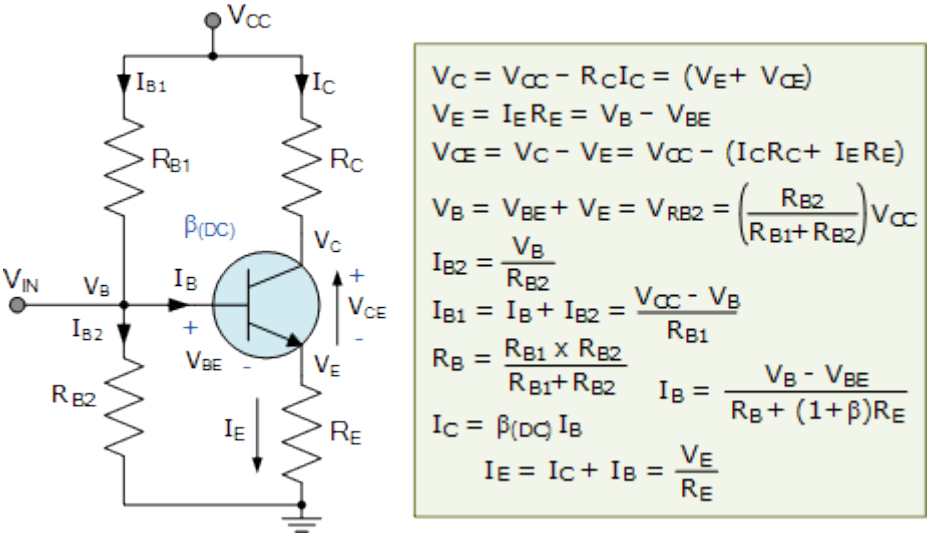
$V_C = V_{CC} - (I_C R_C)$
$V_{CE} = V_C - V_E$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_{CC} - V_{BE}}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

Fig. 1: Fixed bias



$V_C = V_{CC} - I_C R_C$
$V_{CE} = V_{CC} - V_{CE} - I_C(R_C + R_E)$
$V_E = I_E R_E - V_{EE}$
$V_B = V_{BE} + V_E$
$V_{EE} = I_B R_B + V_{BE} + I_E R_E$
$I_C = \beta_{(DC)} I_B$
$I_E = I_C + I_B \approx I_C$

Fig. 2: Emitter bias



$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$$
$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}} \qquad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

Fig. 3: Voltage divider bias

PROCEDURE:

1. Connect the fixed bias circuit as shown in figure 1.
2. Note the DC conditions i.e, the values of VBE, IB and VCE, IC. Calculate β (dc) and the stability factor as mentioned in theory.
3. Heat the transistor by placing a soldering iron in its vicinity for a minute. Note the values of IC and IB.
4. Calculate the stability factors practically and compare them with the theoretical values.
5. Apply input Vin by using function generator to the circuit. Set source voltage as 100mV P-P at 100 Hz frequency using the function generator.
6. Observe the output waveform on CRO and draw the input-output waveform.
7. Repeat the above steps for emitter bias (fig 2) and self bias (fig 3).

CALCULATION:

Biasing Method	Resistance Value (Ω)	β (dc) =Ic/I_B	Stability factor Theoretical
Fixed bias	-		S = 1 + β =
Emitter bias	RB= , RE=		S =(1+β)*(RB+RE)/{RB+(1+β)RE} =
Voltage divider bias	RB1= ,RB2= ,RE=		S =(1+β)*(1+RB/RE)/(1+β+RB/RE) Where RB =(RB1*RB2)/(RB1+RB2) =

Biasing Method	I_B		Ic		Δ I_B /Δ Ic	S = (1+β)/ {1−β(Δ I_B /Δ Ic)}	S Theoretical
	I_B1	I_B2	Ic1	Ic2			
Fixed bias							
Emitter bias							
Voltage divider bias							

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

CONCLUSION:

The different biasing methods of BJT have been studied and the output waveform of in each case has been drawn. It is concluded that the voltage divider biasing method is the best method as the stability factor is lowest.

EXPERIMENT NO – 7

AIM OF THE EXPERIMENT:

Study the single stage CE amplifier and find gain.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS/	SPECIFICATION	QUANTITY
1.	Transistor	BC547	1 No
2.	Resistor	74K, 15K, 4.7K, 1K, 2.2K, 8.2K ohm	1 each
3.	Capacitor	10µF,100µF, 1 KPF	1 each
4.	Dual DC power supply pack	0-30 V	1 pc
5.	CRO with probes		1 pc
6.	Function generator	(0-1)MHz	1 pc
7.	Digital Ammeter	0-200mA	1 No
8.	Digital Voltmeter	0-20 V	1 No
9.	Bread board		1 No
10.	Connecting Wire		As Per Required

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- Vceo max= 50V
- VEB0 = 6V
- VCB0 = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 0C
- hfe = 110 - 220

THEORY:

An amplifier is an electronic circuit that can increase the strength of a weak input signal without distorting its shape. The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification with 180^0 phase shift. The factor by which the input signal gets multiplied after passing through the amplifier circuit is called the gain of the amplifier. It is given by the ratio of the output and input signals.

Gain = output signal / input signal

A self bias circuit is used in the amplifier circuit because it provides highest Q-point stability among all the biasing circuits. Resistors R1 and R2 forms a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region. In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region.

The Bypass Capacitor: The emitter resistor is required to obtain the DC quiescent stability. However the inclusion of it in the circuit causes a decrease in amplification. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC

quiescent condition. Hence capacitor is connected in parallel with emitter resistance which increases the A.C gain.

The Coupling capacitor: An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

Frequency response: The plot of gain versus frequency is called as frequency response. The coupling and bypass capacitors causes the gain to fall at low frequency region and internal parasitic capacitance and shunt capacitor causes the gain to fall at high frequency region. In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appear in the mid frequency range. Hence the mid band frequency gain is maximum. Hence we get a Band Pass frequency response

Characteristics of CE Amplifier:

- Large current gain.
- Large voltage gain.
- Large power gain.
- Current and voltage phase shift of 180°.
- Moderate output resistance.

FOR INPUT CHARACTERISTICS OF CE AMPLIFIER:-

It is the curve between the input biasing voltage [VBE] and input current [IB] at constant Output biasing voltage VCE where, VBE= Base Emitter voltage

IB= Base current

VCE= Collector Emitter voltage

FOR OUTPUT CHARACTERISTICS OF CE AMPLIFIER:-

It is the curve between output biasing voltage [VCE] and output current [IC] at constant input current [IB] where, VCE= Collector Emitter voltage

IC= Collector current

IB= Base current

CIRCUIT DIAGRAM:

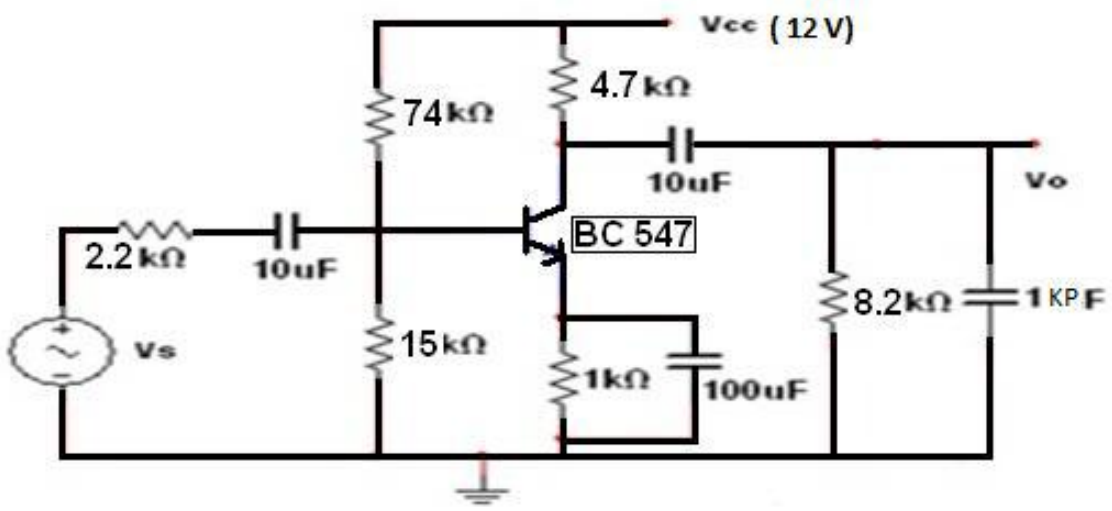


Fig. 1: CE BJT amplifier

PROCEDURE:

1. Connect the circuit as shown in fig.1, Set source voltage as 50mV P-P at 100 Hz frequency using the function generator.
2. Keeping the input voltage as constant, vary the frequency from 100 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage.
3. Plot the graph for gain in (dB) verses Frequency on a semi log graph sheet.
4. Calculate the bandwidth from the graph.

OBSERVATION:

Frequency	Vs (V)	Vo (V)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Graph:

In the usual application, mid band frequency range is defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as fL, fH and are called as the 3dB frequencies or simply the lower and higher cut off frequencies respectively. The difference between the higher cut off and lower cut off frequency is referred to as the bandwidth (fH - fL).

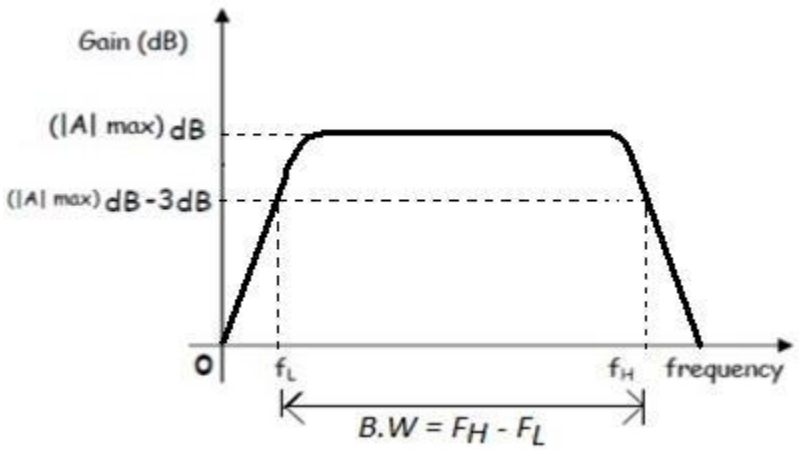


Fig. 2: Frequency Response Curve of RC coupled BJT CE Amplifier

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULTS:

1. The BJT CE amplifier is studied
2. The frequency response curve of the BJT CE amplifier is plotted.
3. Lower cutoff frequency, fL = …….
   Higher cutoff frequency, fH = ……
   Bandwidth = fH – fL = ……
4. Gain of amplifier =

EXPERIMENT NO – 8

AIM OF THE EXPERIMENT:

Study multistage R-C coupled amplifier and determine frequency response and gain.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	R-C coupled amplifier kit		1 No
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

THEORY:

This is the most popular type of coupling because it is cheap and provides excellent audio fidelity over a wide range of frequency. It is usually employed for voltage amplification. As the coupling from one stage to next stage is achieved by coupling of Rc and Cc, therefore such amplification are called R-C coupling amplifier.

When ac signals is applied to the base of the first transistor. It appears in the amplified form across its collector load Rc. The amplified signal developed across Rc is given to the base of the next stage through coupling capacitor Cc. Then the second stage further amplifies the signal and so on. It may be mentioned that the total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the effective load resistance of the first stage is reduced due to shunting effect of the input resistance of the second stage. This reduces the gain of the stage, which is loaded by the next stage.

The coupling does not affect the Q point of the next stage since the Cc blocks the dc voltage of the first stage from reaching the base of the second stage or output. The function of Cin is to couple the signal source Vs to the base of the transistor. At the same time it prevents the dc current of Vcc from reaching the signal source Vs and also prevents any dc component present in Vs from reaching of base. The bypass capacitor C_E is used to prevent the loss of gain due to negative feedback across the resistor R_E. Resistors R1, R2, and R_E are used to bias and stabilize the transistor so that the operating point lie on the middle of the dc load line. The resistor Rc acts as ac load for the amplifier. The RC network is broadband in nature. Therefore, it gives a wideband frequency response and hence used to cover AF range of amplifier. The R-C coupled amplifier has low voltage and power gain and poor impedance matching.

CIRCUIT DIAGRAM:

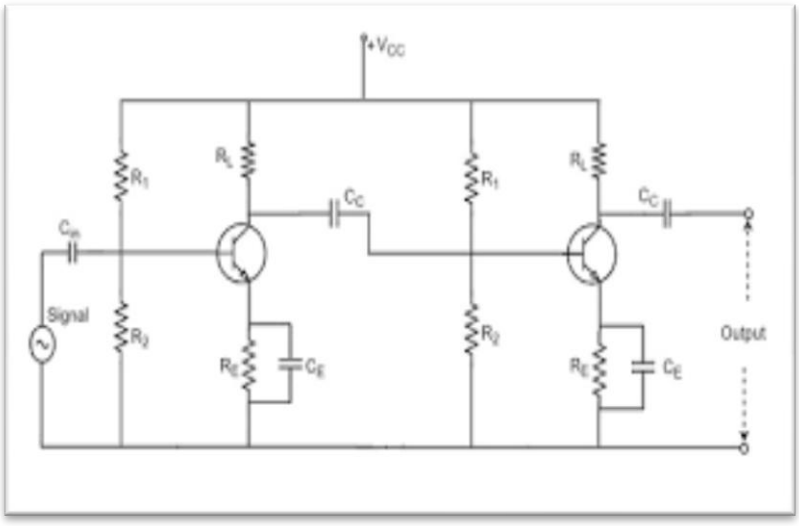


Fig. 1: Two stage R-C coupled amplifier

PROCEDURE:

1. Connect the circuit as shown in fig 1. Apply input by using function generator to the circuit. Set source voltage as 50mV P-P at 100 Hz frequency using the function generator.
2. Observe the output waveform on CRO. Measure the voltage at Output of first stage & second stage.
3. From the readings, calculate voltage gain of first stage, second stage and overall gain of two stages.
4. Disconnect second stage and then measure output voltage of first stage, calculate voltage gain.
5. Compare it with voltage gain obtained when second stage was connected.
6. Keeping the input voltage as constant, vary the frequency from 100 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage. Note down various values of gain for different frequencies.
7. A graph is plotted between frequency and voltage gain on a semi log graph sheet.
8. Calculate the bandwidth from the graph.

OBSERVATION:

Frequency (Hz)	Vs (V)	Vo (V)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

GRAPH:

Frequency response curve is obtained by plotting a graph between frequency and gain in db .The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor Cc and at high frequencies due to junction capacitance Cbe. The lower and higher cuts off frequencies are shown as fL, fH and are called as the 3dB frequencies. The difference between the higher cut off and lower cut off frequency is referred to as the bandwidth (fH - fL).

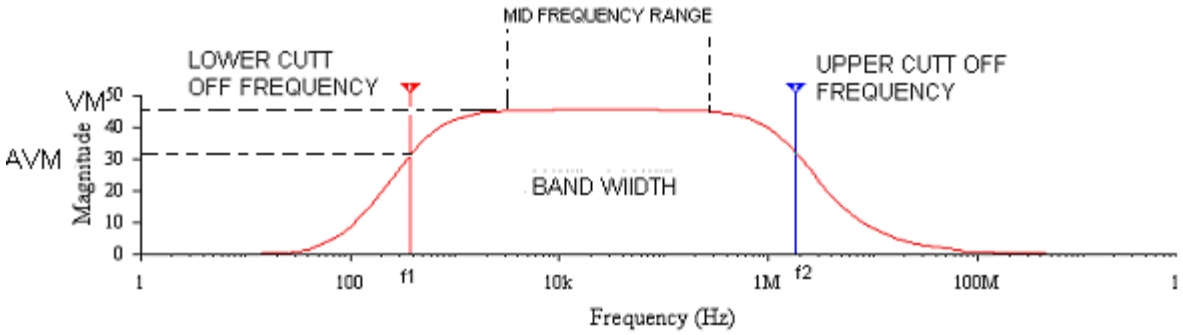


Fig. 2: Frequency Response Curve of RC coupled BJT CE Amplifier

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULTS:

1. The multistage R-C coupled amplifier is studied.
2. The frequency response curve of the R-C coupled amplifier is plotted.
3. Lower cutoff frequency, fL = …….
   Higher cutoff frequency, fH = ……
   Bandwidth = fH – fL = ……
4. Gain of first stage amplifier =
   Gain of second stage amplifier =
   Overall Gain of two stage amplifier =

EXPERIMENT NO – 9

AIM OF THE EXPERIMENT:

Construct and find the gain of class- A, class- B and class -C amplifier.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Class A, B & C power amplifier kit		1 No
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

THEORY:

The power amplifiers are generally classified into:-

1) Class A power Amplifier
2) Class B power Amplifier
3) Class C power Amplifier

The classes are based on the proportion of each input cycle (conduction angle) during which an amplifying device passes current.

Class A power Amplifier:-

In this amplifier, the collector current flows for full cycle of the input ac signal. This type of amplifier is the most common type of amplifier topology as it uses just one output switching transistor (Bipolar, FET, IGBT, etc). This single output transistor is biased around the Q-point within the middle of its load line and so is never driven into its cut-off or saturation regions, thus allowing it to conduct current over the full 360 degrees of the input cycle. Then the output transistor of a class-A topology never turns "OFF" which is one of its main disadvantages. The class A amplifier is equivalent to a current source. In this amplifier the output power is low, so the efficiency is about 35%.

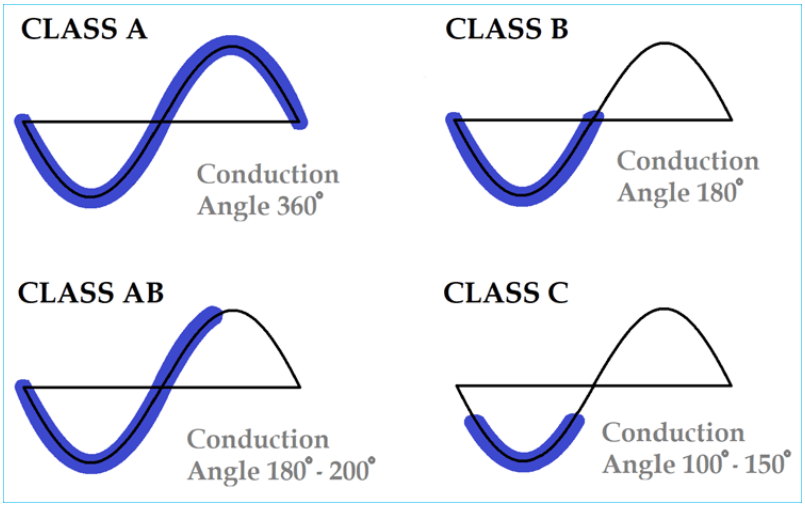
Class B power Amplifier:-

In this amplifier, the collector current flows for positive half cycle of the input ac signal and do not flow for the negative half cycle of the input ac signal. During positive half cycle of input signal, E-B junction is forward biased and collector current flows. During negative half cycle, E-B junction is reverse biased and collector current does not flow. In this amplifier the output power is higher, so the efficiency is about 50% - 60% and thus this amplifier is mostly used as power amplifier. **Class B amplifiers** were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform. Class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

Class C power Amplifier:-

In this amplifier, the collector current flows for less than half cycle of the input ac signal. Such amplifiers are never used for power amplification and used as tuned amplifier. This amplifier's efficiency is about 78% - 80%. It has the greatest efficiency but the poorest linearity. The previous classes, A, B and AB are considered linear amplifiers, as the output signals amplitude and phase are linearly related to the input signals amplitude and phase. Class C amplifiers are commonly used in high frequency sine wave oscillators.

The basic difference in all types of power amplifier is:-



CIRCUIT DIAGRAM:

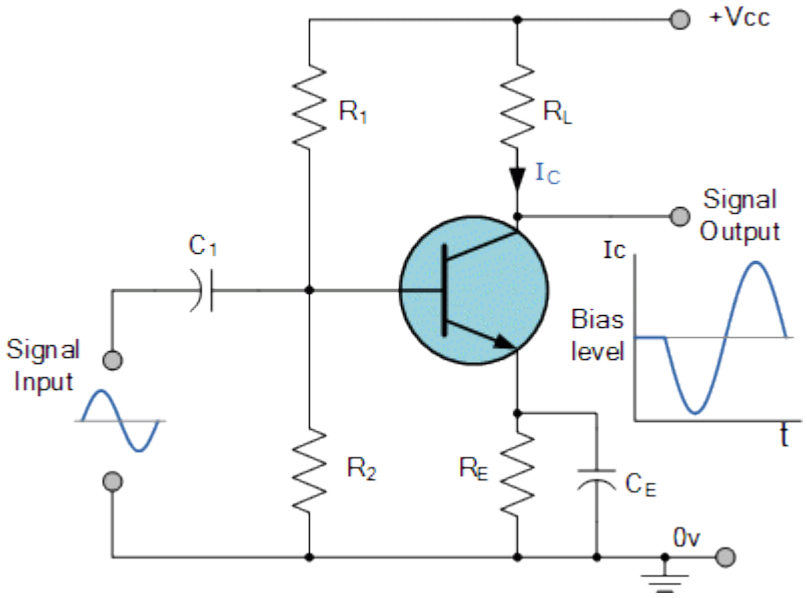


Fig. 1: Class A amplifier

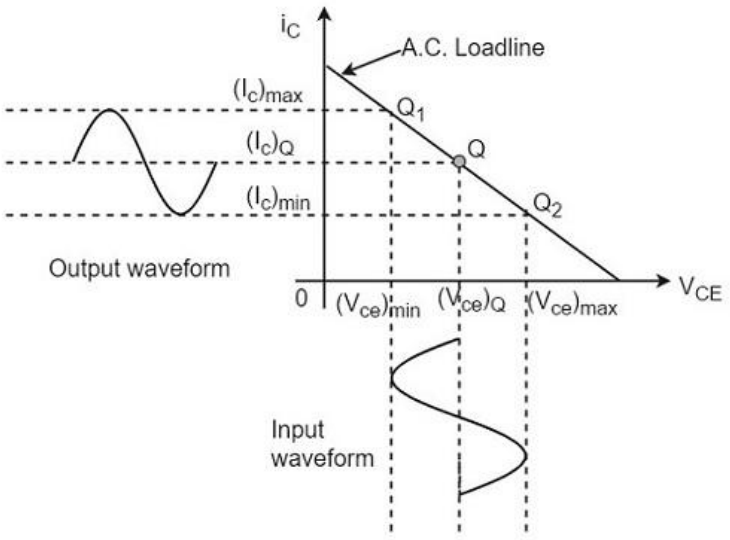


Fig. 2: output waveform of Class A amplifier

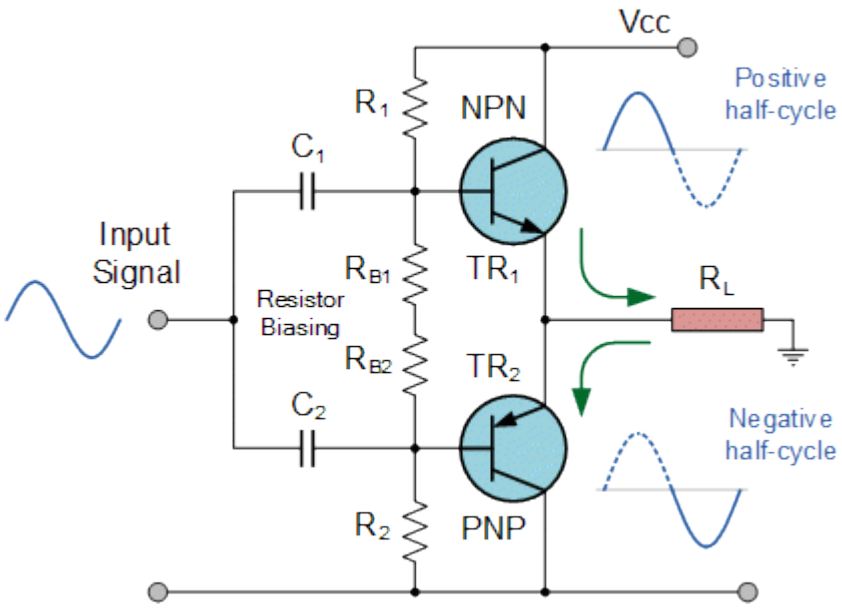


Fig. 3: Class B amplifier

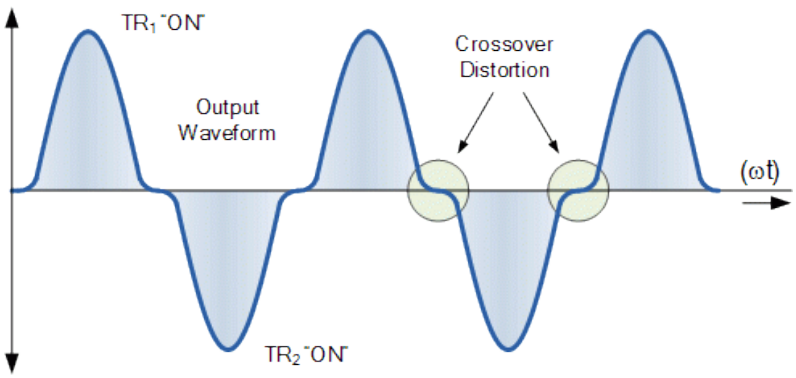


Fig. 4: output waveform of Class B amplifier

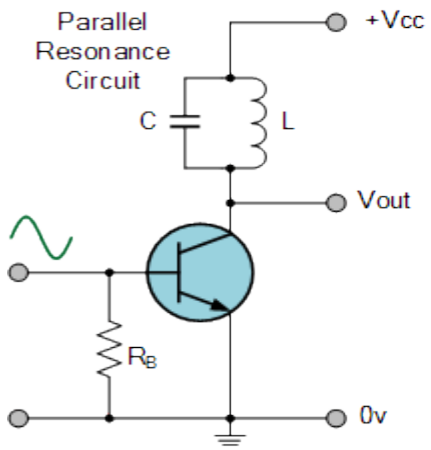


Fig. 5: Class C amplifier

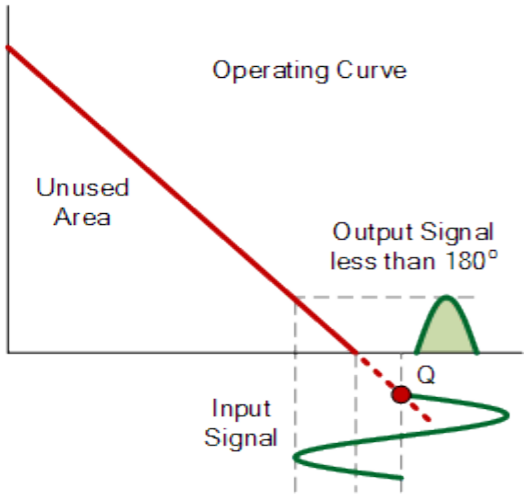


Fig. 6: Output waveform of Class C amplifier

PROCEDURE:

1. Connect the circuit as shown in fig.1, Set source voltage as 100mV P-P at 100 Hz frequency using the function generator.
2. Keeping the input voltage as constant, vary the frequency from 100 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage.
3. Plot the graph for gain in (dB) verses Frequency on a semi log graph sheet.
4. Repeat the above steps for Class B amplifier (fig 3) and Class C amplifier (fig 5).

TABULATION:

Amplifier	Freq (Hz)	Vs (V)	Vo (V)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)
CLASS A					
CLASS B					
CLASS C					

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULTS:

Gain of Class A amplifier =
Gain of Class B amplifier =
Gain of Class C amplifier =

EXPERIMENT NO – 10

AIM OF THE EXPERIMENT:

Construct and test push pull amplifier and observe waveform.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Push pull amplifier kit		1 No
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

THEORY:

Different types of push pull amplifiers, like Class A, Class B and Class AB push pull amplifier can be designed. A push pull amplifier is an amplifier which has an output stage that can drive a current in either direction through the load. The output stage of a typical push pull amplifier consists of two identical BJTs or MOSFETs one sourcing current through the load while the other one sinking the current from the load. Push pull amplifiers are superior over single ended amplifiers (using a single transistor at the output for driving the load) in terms of distortion and performance. A single ended amplifier, how well it may be designed will surely introduce some distortion due to the non linearity of its dynamic transfer characteristics. Push pull amplifiers are commonly used in situations where low distortion, high efficiency and high output power are required. The basic operation of a push pull amplifier is as follows: The signal to be amplified is first split into two identical signals 180° out of phase. Generally this splitting is done using an input coupling transformer. The input coupling transformer is so arranged that one signal is applied to the input of one transistor and the other signal is applied to the input of the other transistor. Advantages of push pull amplifier are low distortion, absence of magnetic saturation in the coupling transformer core, and cancellation of power supply ripples which results in the absence of hum while the disadvantages are the need of two identical transistors and the requirement of bulky and costly coupling transformers.

Class A push pull amplifier- The circuit diagram of a typical Class A push pull amplifier is shown in fig 1. Quiescent current of Q2 and Q1 flows in opposite directions through the corresponding halves of the primary of T2 and as a result there will be no magnetic saturation. The phase splitted signals being applied to the base of each transistor. When Q1 is driven positive using the first half of its input signal, the collector current of Q1 increases. At the same time Q2 is driven negative using the first half of its input signal and so the collector current of Q2 decreases. The collector currents of Q1 and Q2 i.e. I1 and I2 flows in the same direction through the corresponding halves of the T2 primary. As a result an amplified version of the original input signal is induced in the T2 secondary. It is clear that the current through the T2 secondary is the difference between the two collector currents.

Class B push pull amplifier- The Class B push pull amplifier is almost similar to the Class A push pull amplifier and the only difference is that there is no biasing resistors for a Class B push pull amplifier. This means that the two transistors are biased at the cut off point. The Class B configuration can provide better power output and has higher efficiency (up to 78.5%). The input signal is converted

into two similar but phase opposite signals by the input transformer T1. One out of these two signals is applied to the base of the upper transistor while the other one is applied to the base of the other transistor. When transistor Q1 is driven to the positive side using the positive half of its input signal, the reverse happens in the transistor Q2. That means when the collector current of Q1 is going in the increasing direction, the collector current of Q2 goes in the decreasing direction. Anyway the current flow through the respective halves of the primary of the T2 will be in same direction. This current flow through the T2 primary results in a wave form induced across its secondary. The wave form induced across the secondary is similar to the original input signal but amplified in terms of magnitude. Cross over distortion is a type of distortion commonly seen in Class B amplifier configurations.

CIRCUIT DIAGRAM:

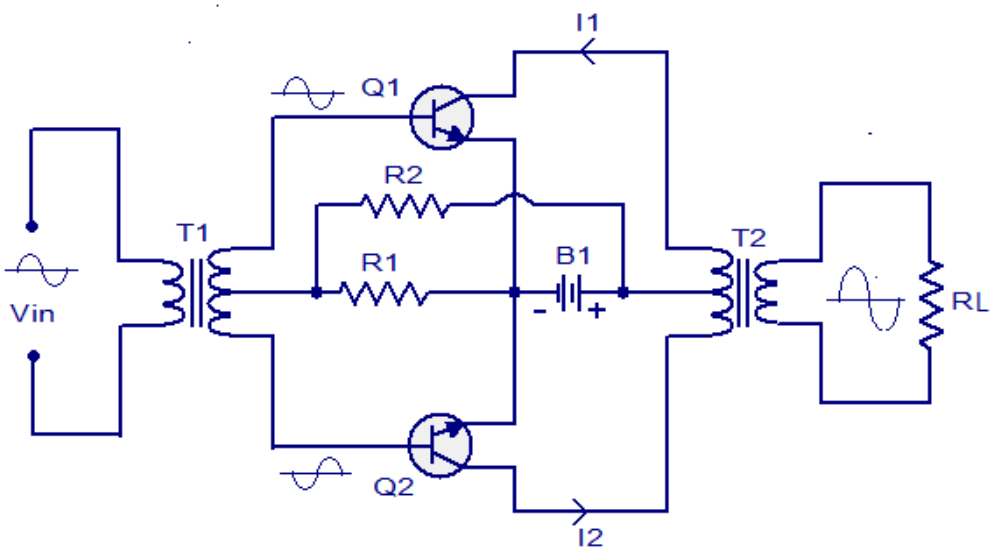


Fig. 1: Class A push pull amplifier

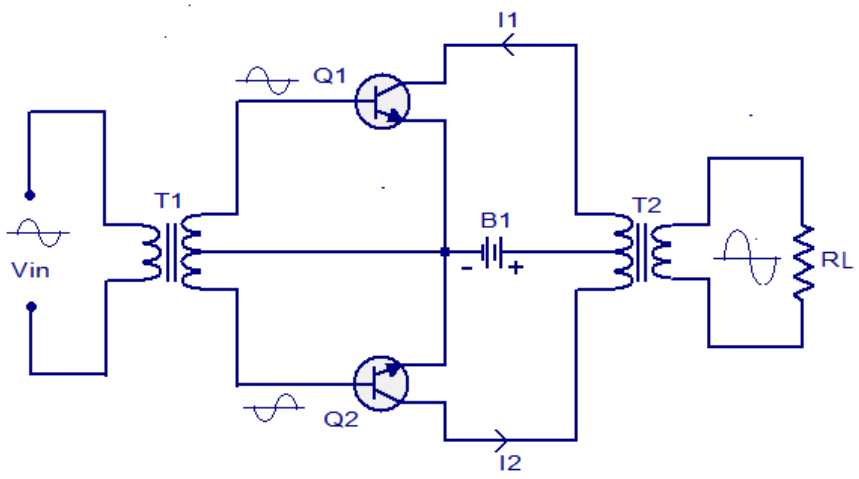


Fig. 2: Class B push pull amplifier

PROCEDURE:

1. Connect the circuit as per the circuit diagram fig 1.
2. Apply 1V p-p with 1KHZ frequency using function generator.
3. Observe the output in CRO.
5. Remove the collector connection and put ammeter.
6. Note the Idc value in the ammeter.
7. Using Pdc and Pac formulas, find the efficiency.
8. Repeat the same for fig 2. Note the cross over distortion in output.

OBSERVATION:

$Pac=Vm^2/2\ R_L'= Vcc^2/2\ R_L'$

R_L' = [N1 / N2] ^{2} R_L where N1 & N2 are the turns of primary & secondary winding of output transformer

$Pdc=Vcc*Idc = Vcc \times(2\ Im/\ \pi)$

EFFICIENCY (η) =(Pac/Pdc)*100

Amplifier	Vcc (V)	Turns ratio (N1/N2)	$R_L' = [N1/N2]^2 R_L$	Idc (mA)	Pac= $Vcc^2/2\ R_L'$	Pdc= Vcc*Idc	η = (Pac/Pdc)*100
Class A push pull							
Class B push pull							

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULTS:

The ouput waveform of class A & class B push pull amplifier is observed and drawn.
Efficiency of class A push pull amplifier =
Efficiency of class B push pull amplifier =

EXPERIMENT NO – 11

AIM OF THE EXPERIMENT:

Construct (i) Hartley oscillator (ii) Colpitts oscillator (iii) Wein bridge oscillator (iv) R-C phase shift oscillator and draw waveform & calculate the frequency.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Different Oscillator kit		1 No each
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

THEORY:

An Oscillator is an electronic circuit that provides an AC output without using an AC input. All sinusoidal oscillator circuits use the concept of positive feedback to produce oscillations. An oscillator circuit must satisfy the Barkhausen's criteria of unity loop gain to produce oscillations. Oscillators are extensively used in radio & TV receivers to generate a high frequency carrier signal in the tuning stages. Frequency of oscillations is the frequency at which the phase of loop gain equals zero or integral multiple of 2π. Oscillations are sustained when the magnitude of loop gain equals unity.

Type of Oscillator Frequency Ranges:

Wien bridge oscillator		1 Hz	—	1 MHz
Phase shift oscillator		1 Hz	—	10 MHz
Hartley oscillator		10 kHz	—	100 MHz
Colpitt's oscillator		10 kHz	—	100 MHz
Negative resistance oscillator		> 100 MHz		
Crystal oscillator		Fixed frequency		

In a Hartley oscillator, the oscillation frequency is determined by a tank circuit comprising of two inductors L1, L2 and one capacitor C1. Feedback to the base of transistor is taken from the junction of Capacitor C1 and inductor L2 in the tank circuit. Frequency of the Hartley oscillator is given by-

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Where, C is the capacitance of the capacitor C1 in the tank circuit and L=L1+L2+2M where M is the mutual inductance between the two coils.

In a Colpitts oscillator, the oscillation frequency is determined by a tank circuit comprising of one inductor L1 and two capacitor C1, C2. Feedback to the base of transistor is taken from the junction of Capacitor C2 and inductor L1 in the tank circuit. Frequency of the Colpitts oscillator is given by-

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Where, C is the effective capacitance in the tank circuit. C = (C1C2)/(C1+C2) and L is the inductance of the inductor L1 in the tank circuit.

Due to the excellent performance in the high frequency region, the Colpitts oscillator can be even used in microwave applications.

Wein bridge oscillator comprises of a two-stage amplifier with an R-C bridge circuit. R-C bridge circuit (Wien bridge) is a lead-lag network. The phase'-shift across the network lags with increasing frequency and leads with decreasing frequency. In the bridge circuit R_1 in series with C_1, R_3, R_4 and R_2 in parallel with C_2 form the four arms. This bridge circuit can be used as feedback network for an oscillator, provided that the phase shift through the amplifier is zero. This requisite condition is achieved by using a two stage amplifier. In this arrangement the output of the second stage is supplied back to the feedback network and the voltage across the parallel combination C_2 R_2 is fed to the input of the first stage. Transistor Q_1 serves as an oscillator and amplifier whereas the transistor Q_2 as an inverter to cause a phase shift of 180°. The circuit uses positive and negative feedbacks. The positive feedback is through R_1 C_1 R_2, C_2 to transistor Q_1 and negative feedback is through the voltage divider to the input of transistor Q_1. Resistors R_3 and R_4 are used to stabilize the amplitude of the output. The two transistors Q_1 and Q_2 thus cause a total phase shift of 360° and ensure proper positive feedback. The negative feedback is provided in the circuit to ensure constant output over a range of frequencies. This is achieved by taking resistor R_4 in the form of a temperature sensitive lamp, whose resistance increases with the increase in current. In case the amplitude of the output tends to increase, more current would provide more negative feedback. Thus the output would regain its original value. A reverse action would take place in case the output tends to fall.

The generalized expression for the frequency of oscillations produced by a RC phase-shift oscillator is given by

$$f_r = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

$$if\ R_1 = R_2 = R\ and\ C_1 = C_2 = C$$

$$then\ f_r = \frac{1}{2\pi RC}$$

Advantages

1. Provides a stable low distortion sinusoidal output over a wide range of frequency and high gain.
2. The frequency range can be selected simply by using decade resistance boxes.

RC phase shift oscillator or simply RC oscillator is a type of oscillator where a simple RC network (resistor-capacitor) network is used for giving the required phase shift to the feedback signal. Mathematically the phase angle of the RC network is expressed as

$$\varphi = tan^{-1}\frac{X_C}{R}$$

RC phase-shift oscillator1 is formed by cascading three RC phase-shift networks, each offering a phase-shift of 60^o. The generalized expression for the frequency of oscillations produced by a RC

phase-shift oscillator is given by

$$f = \frac{1}{2\pi RC\sqrt{2N}}$$

Where, N is the number of RC stages formed by the resistors R and the capacitors C.

Advantages

1. Provides excellent frequency stability.
2. The RC oscillator can output a pure sine wave on a wide range of loads.

CIRCUIT DIAGRAM:

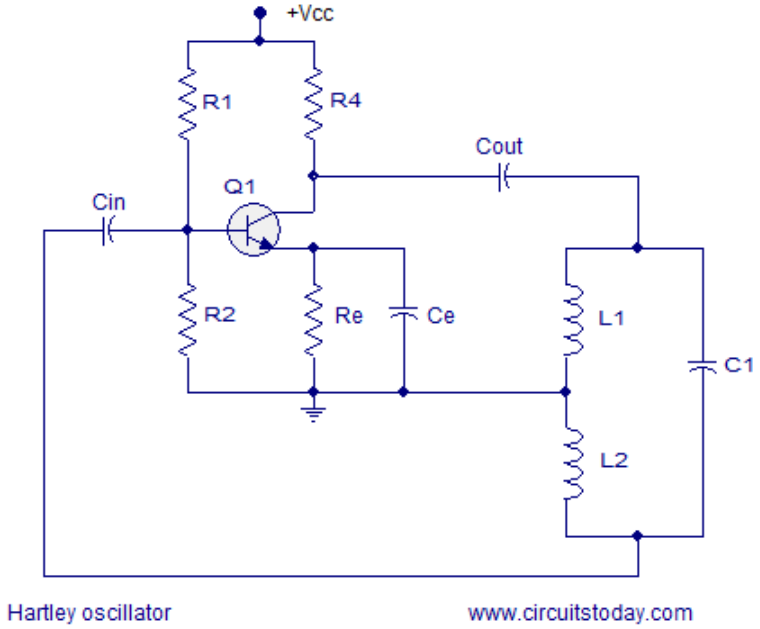


Fig. 1: Hartley oscillator

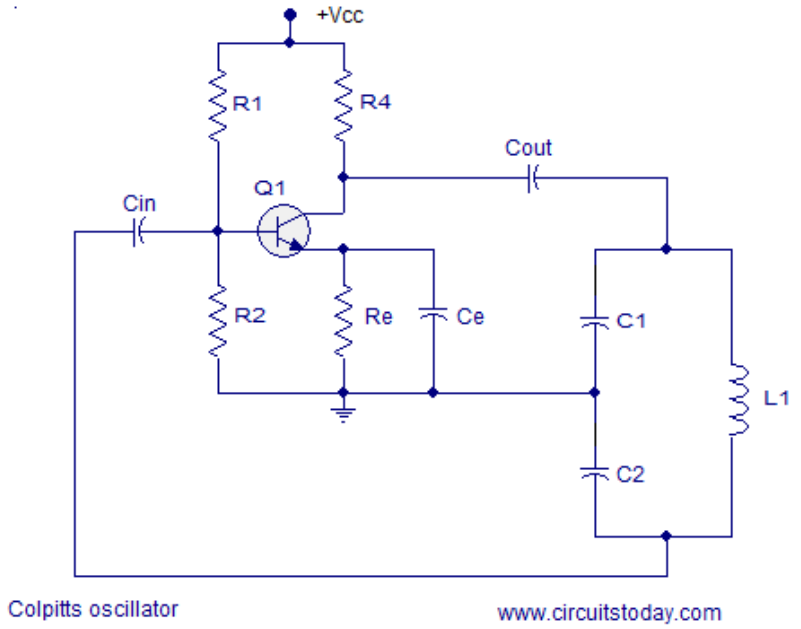


Fig. 2: Colpitt's oscillator

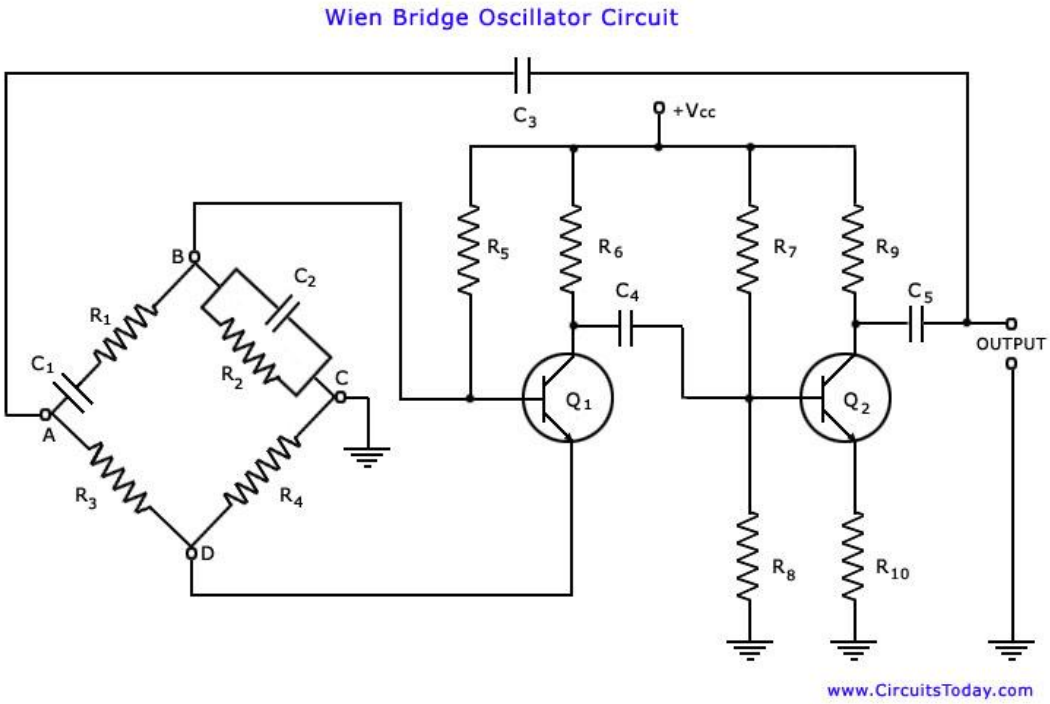


Fig. 3: Wein bridge oscillator

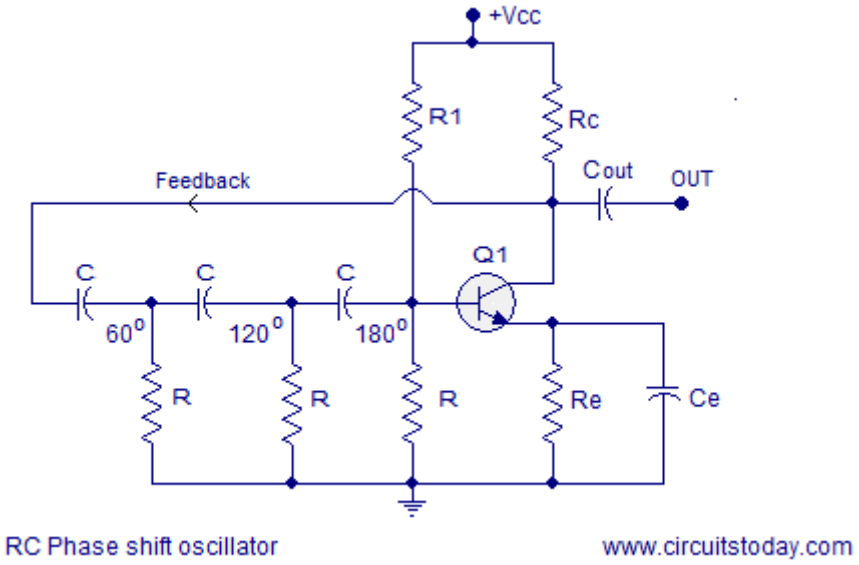


Fig. 4: R-C phase shift oscillator

PROCEDURE:

Hartley Oscillator-

1) Complete the circuit as shown in Fig. 1, by connecting the capacitor C1 provided on panel of the trainer.
2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & vary the Rc till the stable oscillations are obtained on the CRO.
4) Now measure the frequency of oscillations practically.
5) Draw the oscillations obtained on a graph sheet.

Colpitts Oscillator-

1) Complete the circuit as shown in Fig. 2, by connecting the capacitors C1 & C2 provided on panel of the trainer.
2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & measure the frequency of oscillations practically.
4) Draw the oscillations obtained on a graph sheet.

Wein bridge Oscillator-

1) Complete the circuit as shown in Fig. 3, by connecting the R-C bridge provided on panel of the trainer.
2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & measure the frequency of oscillations practically.
4) Draw the oscillations obtained on a graph sheet.

R-C phase shift Oscillator-

1) Complete the circuit as shown in Fig. 3, by connecting the R-C network provided on panel of the trainer.
2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & measure the frequency of oscillations practically.
4) Draw the oscillations obtained on a graph sheet.

CALCULATIONS:

Oscillator	Theoretical value of frequency of oscillation (Hz)	Practical value of frequency of oscillation (Hz)
Hartley		
Colpitts		
Wein bridge		
R-C phase shift		

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
3. Make sure while selecting the emitter, base and collector terminals of the transistor.
4. Do not touch the capacitor terminals.

CONCLUSION:

The operation of Hartley, Colpitts, Wein Bridge and R-C phase shift oscillator circuits are studied and their frequency of oscillations is verified with the theoretical values.

EXPERIMENT NO – 12

AIM OF THE EXPERIMENT:

To construct and test Differentiator and Integrator using R-C circuit.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPARATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Opamp differentiator/integrator kit		1 No
2.	Dual DC power supply pack	0-30 V	1 pc
3.	CRO with probes		1 pc
4.	Function generator	0-1MHz	1 pc
5.	Connecting Wire		As Per Required

THEORY:

An integrator is a circuit in which the output waveform is the integral of the input waveform. Such a circuit is also termed as integrating amplifier. The circuit is somewhat similar to an opamp inverting amplifier but the feedback resistor Rf is replaced by a capacitor Cf. The circuit diagram of an opamp as an integrator is shown below:

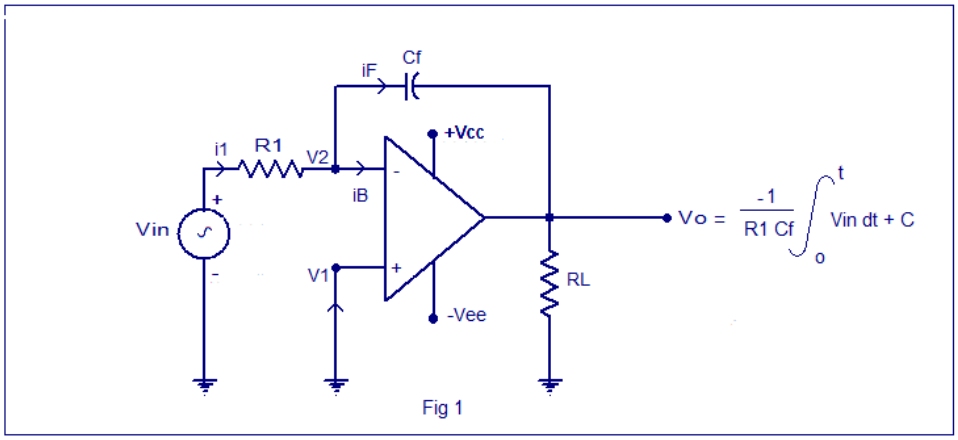


Fig 1

Equation for the instantaneous output voltage of the opamp integrator can be derived as follows:

Applying Kirchoff's current (KCL) at node V2 we get

i1= iF + iB

Since the input resistance of an opamp is very high (in the range of Mega ohms), iB will be very small at it can be neglected. Therefore i1 = iF

The relation between the current through a capacitor and voltage across it is $i_C = C\ dv/dt$.

Therefore $iF = C_f X\ d\ (V_2 – Vo\ ) / dt$

Also $i1 = (Vin – V_2) / R_1$.

Therefore the equation i1 = iF can be rewritten as $(Vin – V_2) / R_1 = C_f X\ d(V_2 – Vo) / dt$…….(1)

Since the non-inverting input is connected to ground, V1 can be taken as 0. Since the open loop gain of the present circuit is near infinity, V2 can be assumed to be zero.

So the equation (1) becomes; Vin / R1 = Cf X d (-Vo) / dt

Integrating the both sides of the above equation with respect to time, we get

$$\int_0^t \text{Vin}/\text{R1} = \int_0^t \text{Cf d (-Vo)} / \text{dt} = \text{Cf (-Vo)} + \text{Vo @ t} = 0$$

Rearranging the equation we get :

$$\text{Vo} = -1 / (\text{R1 Cf}) \text{ X } \int_0^t \text{Vin dt} + \text{C} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Where, C is the integration constant and it has a proportional relationship with the output voltage at time t = 0. From equation (2) it is clear that the output voltage has an inverse relation with the R1 Cf (time constant) and a directly proportional relation with the negative integral of the input voltage.

In the DC condition Cf offers infinite resistance and so the integrator circuit will be like an inverting opamp amplifier with infinite feedback resistance (Rf = ∞). The equation for the voltage gain (A) of an opamp amplifier in inverting mode is A = -(Rf/R1). Substituting Rf=∞ in the present scenario we get A=∞. Therefore the small input offset voltage will get amplified by this factor and there will be an error voltage at the output. This problem can be solved by adding a feedback resistor Rf parallel to Cf as shown in fig 3.

A differentiator is a circuit in which the output waveform is the derivative of the input waveform. Such a circuit is also termed as differentiating amplifier. The circuit is somewhat similar to an opamp inverting amplifier but the input resistor R1 is replaced by a capacitor C1. The circuit diagram of an opamp as a differentiator is shown below:

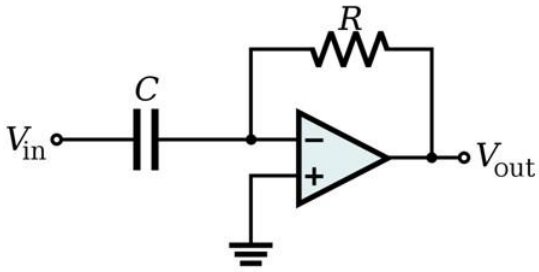


Fig 2

Equation for the instantaneous output voltage of the opamp differentiator can be derived as follows:

Applying Kirchoff's current (KCL) at node V2 we get

ic= iF + iB

Since the input resistance of an opamp is very high (in the range of Mega ohms), iB will be very small at it can be neglected. Therefore ic = iF

The relation between the current through a capacitor and voltage across it is $i_C = C\ dv/dt$.

Therefore ic = C1 X d (Vin – V_2) / dt

Also iF = (V_2 – V_o) / R_F.

Therefore the equation ic = iF can be rewritten as C1 X d (Vin – V_2) / dt = (V_2 – V_o) / R_F …….(1)

Since the non-inverting input is connected to ground, V1 can be taken as 0. Since the open loop gain of the present circuit is near infinity, V2 can be assumed to be zero.

So the equation (1) becomes; (- V_o) / R_F = C1 X d (Vin) / dt

$$\Rightarrow \quad V_o = -R_F\ C1 \text{ X d (Vin)} / \text{dt} \quad \ldots\ldots\ldots(2)$$

From equation (2) it is clear that the output voltage is equal to R_FC1 times the negative instantaneous rate of change of the input voltage with time. It performs the reverse operation of integrator function.

For an ideal differentiator, the gain increases as frequency increases. Thus, at some higher frequencies, the differentiator may become unstable and cause oscillations which results in noise. These problems can be avoided or corrected in a practical differentiator circuit which uses a resistor Rin in series with the input capacitor Cin (or C1) and a capacitor Cf in parallel with the feedback resistor Rf, as shown in the figure 4.

CIRCUIT DIAGRAM:

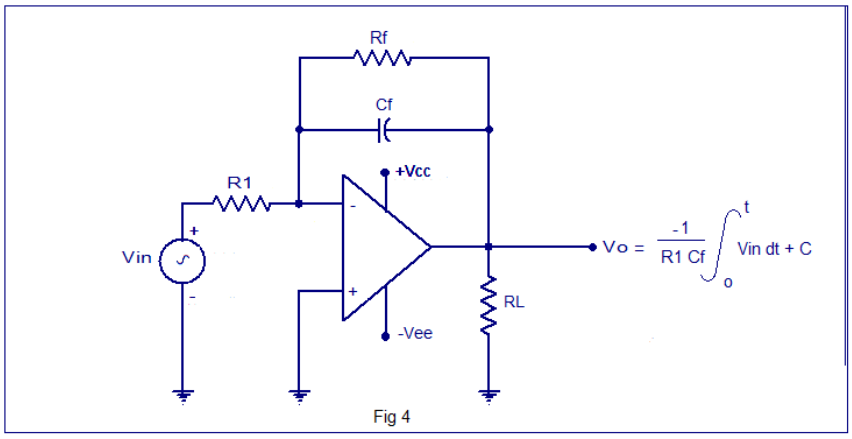


Fig. 3: Practical Integrator

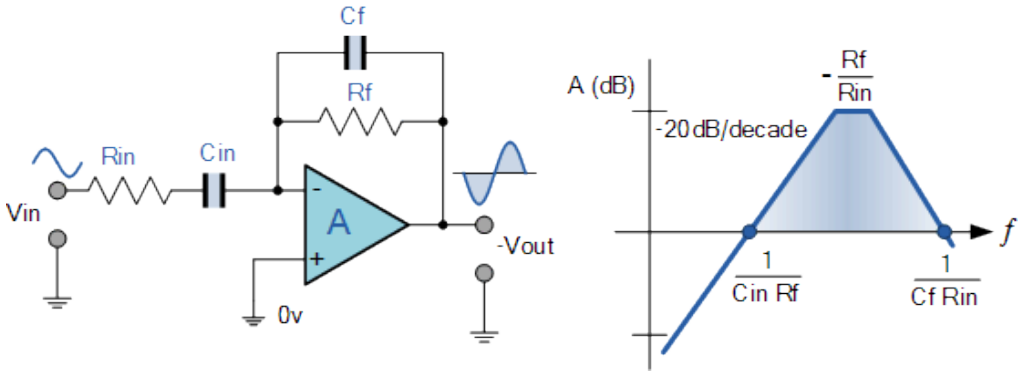


Fig. 4: Practical differentiator

PROCEDURE:

Integrator:

1. Connect the circuit as per the circuit diagram fig 3.
2. Apply square wave and sine wave of 1V p-p with 1KHZ frequency using function generator.
3. Observe the output in CRO.

Differentiator:

1. Connect the circuit as per the circuit diagram fig 4.
2. Apply square wave, triangular wave and sine wave of 1V p-p with 1KHZ frequency using function generator.
3. Observe the output in CRO.

OBSERVATION:

Integrating a square wave will result in a triangle waveform and integrating a sine wave will result in a Cosine waveform.

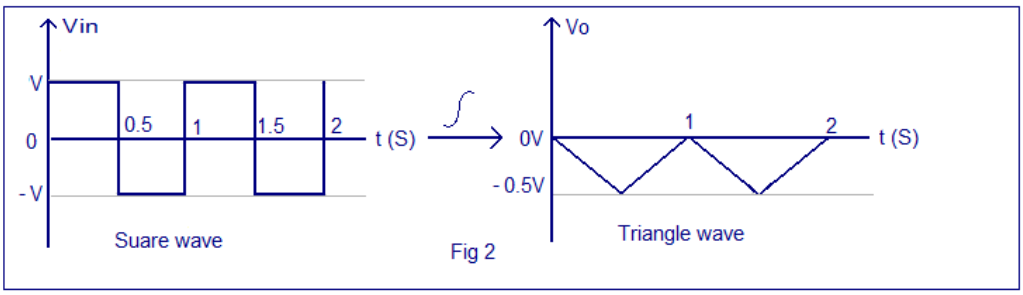


Fig 2

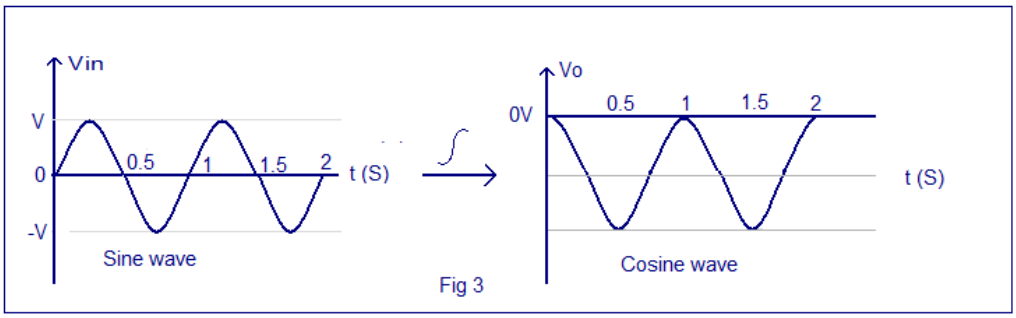
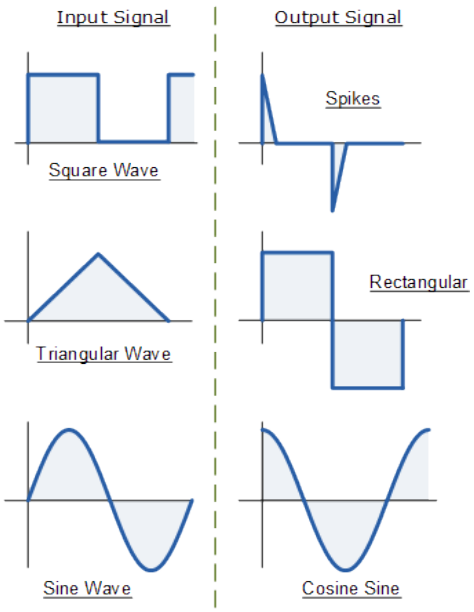


Fig 3

Differentiating a square wave will result in a spike waveform, differentiating a triangular wave will result in a rectangular waveform and differentiating a sine wave will result in a Cosine waveform.



PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the opamp. This may lead to damage the opamp.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting different pins of opamp.

RESULTS:

The ouput waveforms wrt various input of integrator and differentiator are observed and drawn.

EXPERIMENT NO – 13

AIM OF THE EXPERIMENT:

To study about different types of Multivibrators and draw output waveform.

APPARATUS REQUIRED:

SL NO.	NAME OF THE APPRATUS/ COMPONENTS	SPECIFICATION	QUANTITY
1.	Transistor	2N3904/BC507	2 Nos
2.	Resistor	1K, 4.7K, 10K ohm	4 No, 2 No, 2 No
3.	Capacitor	0.1µF, 0.01µF, 1 nF	2 each
4.	Diode	1N4148	2 Nos
5.	Dual DC power supply pack	0-30 V	1 pc
6.	CRO with probes	(0-20) MHz	1 pc
7.	Function generator	(0-1)MHz	1 pc
8.	Bread board		1 No
9.	Connecting Wire		As Per Required

THEORY:

Pulse generators are circuits that generate a pulse waveform directly and most of them use the relaxation principle (charging & discharging of capacitor). The most common type is the multivibrator. Multivibrator is an electronic circuit that generates square waves (or other non-sinusoidals such as rectangular, sawtooth waves). It is a switching circuit which depends for operation on positive feedback. It consists of two stages, resistance coupled amplifier with the output of each stage coupled resistively to the other. Multivibrators are classified into three types:-

(A) Astable multivibrator:-

It is a multivibrator in which stages are switched from ON to OFF state in regular time intervals without any triggering. It is also called free running multivibrator. An astable multivibrator has two quasi-stable states, and it keeps on switching between these two states, by itself. No external triggering signal is needed. The astable multivibrator cannot remain indefinitely in any of these two states. The two amplifiers of an astable multivibrator are regeneratively cross-coupled by capacitor**.** It has no stable state. It is used as relaxation oscillator. The circuit diagram is shown in Fig 1.

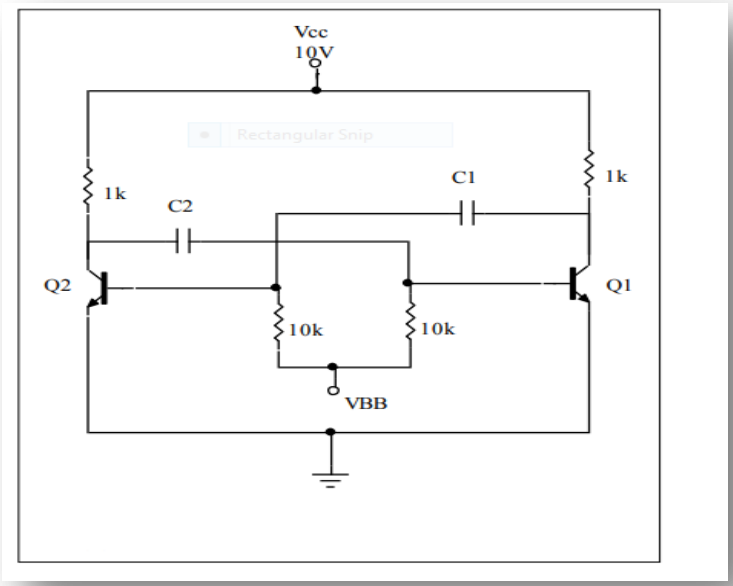
(B) Monostable multivibrator:-

In this case, one stage is ON until it is triggered, in the same time the other stage is made to be ON for a predetermined length of time, and then switched back to its original state automatically. It is also called one shot. A monostable multivibrator has only one stable state, the other state being quasi stable. Normally the multivibrator is in the stable state, and when an external triggering pulse is applied, it switches from the stable to the quasi-stable state. It remains in the quasi-stable state for a short duration, but automatically reverts i.e. switches back to its original stable state, without any triggering pulse". The circuit diagram is shown in Fig 2.

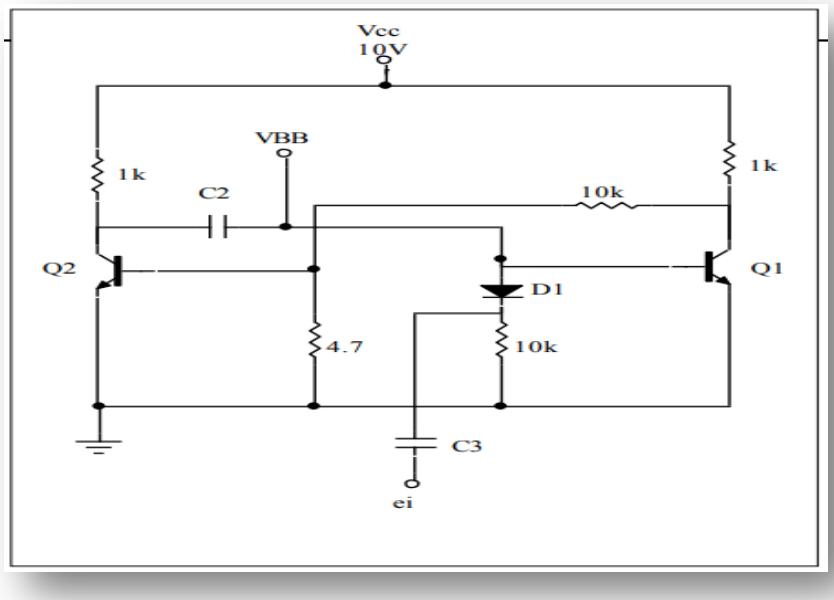
(C) Bistable multivibrator:-

In this case, one stage remains stable in one state (ON or Off) until a triggering pulse is applied to initiate the switching action to reverse the stability condition. A bistable multivibrator has two stable output states. It can remain indefinitely in any one of the two stable states, and it can be induced to make an abrupt transition to the other stable state by means of suitable external excitation. It would remain indefinitely in this stable state, until it is again induced to switch into the original stable state by external triggering. Bistable multivibrators are also termed as Binary‟s or Flip-flops‟**.** It is widely used in digital logic and computer memory. The circuit diagram is shown in Fig 3.

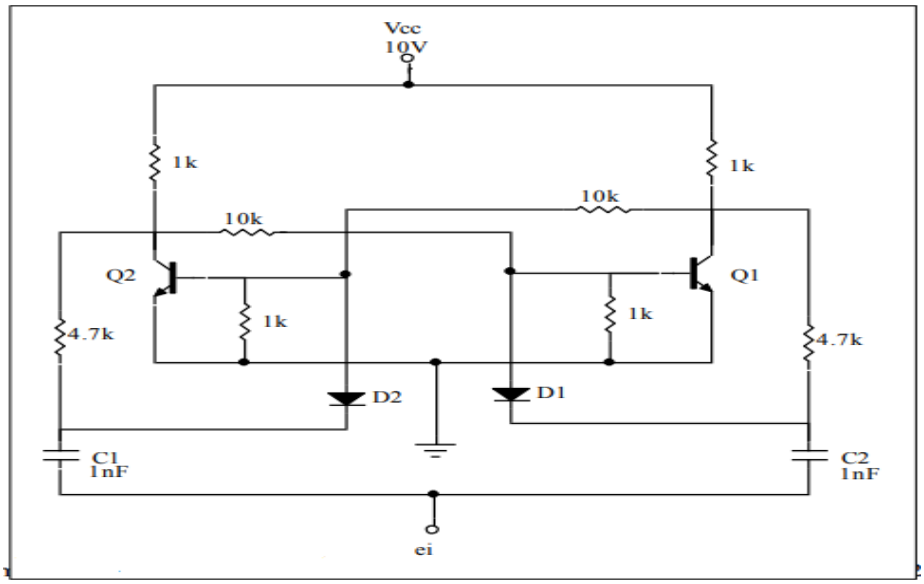
Circuit Diagram:



(Fig 1: Astable Multivibrator)



(Fig 2: Monostable Multivibrator)



(Fig 3: Bistable Multivibrator)

PROCEDURE:

Astable circuit:

1. Connect the circuit as shown in figure 1.
2. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2} and find frequency.
3. Vary C from 0.01 to 0.1μF and measure the frequency at each step.
4. Keep the DC- AC control of the Oscilloscope in DC mode.

Monostable circuit:

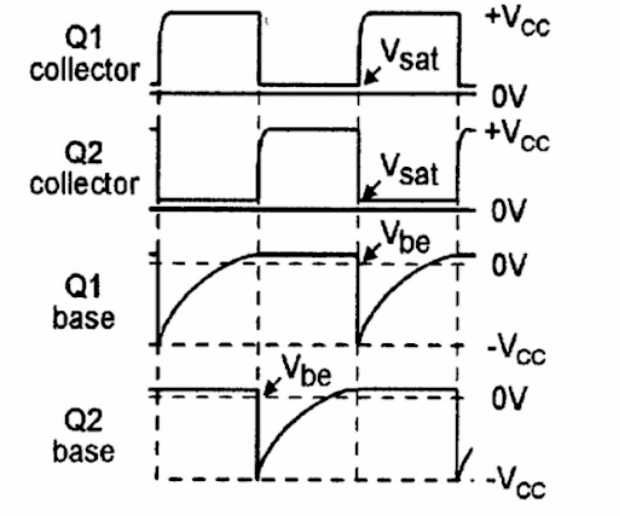
1. Connect the circuit as shown in figure 2.
2. With the help of a triggering circuit and using the condition T (trig) > T(Quasi) a pulse waveform is generated.
3. The output of the triggering circuit is connected to the base of the off transistor.
4. The Off transistor goes into ON state.
5. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2}
6. Keep the DC- AC control of the Oscilloscope in DC mode.

Bistable circuit:

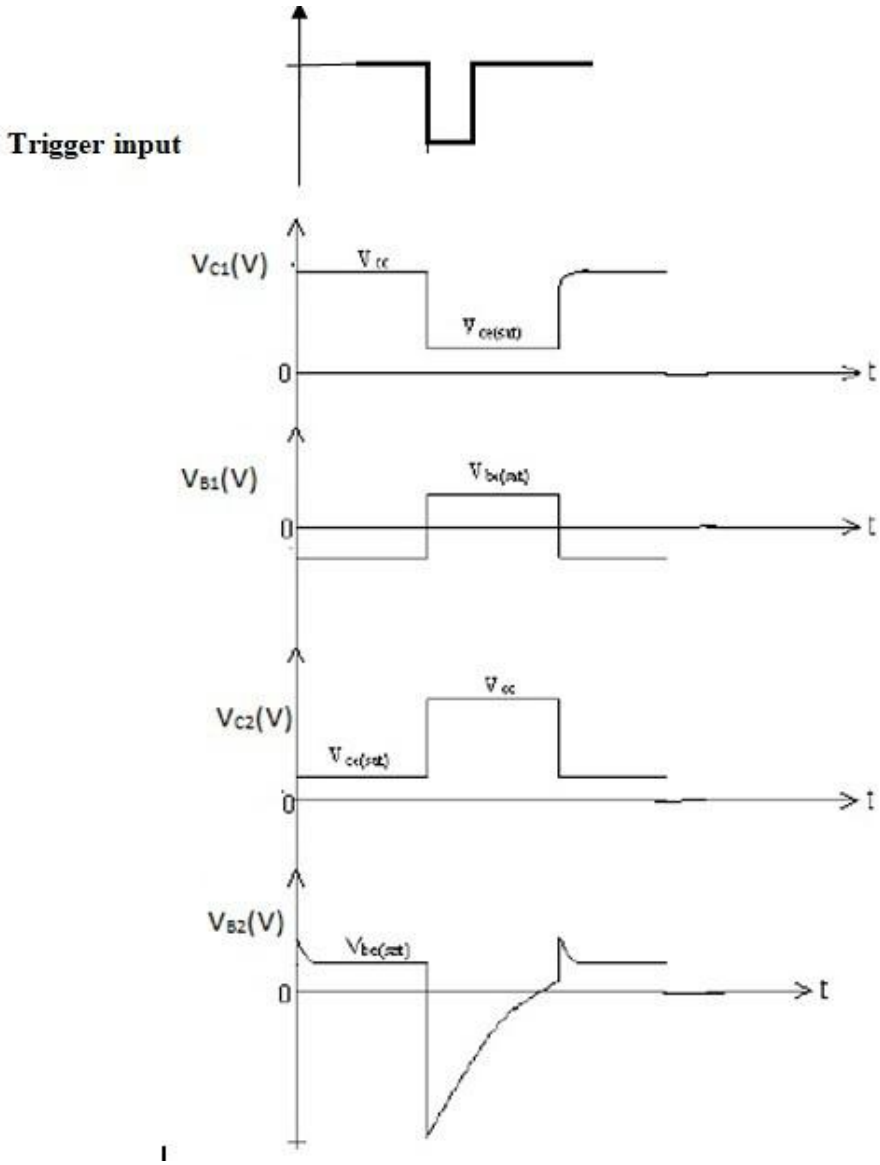
1. Connect the circuit as shown in figure 3.
2. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2}
3. Observe which transistor is in ON state and which transistor is in OFF state.
4. Apply –ve triggering at the base of the ON transistor and observe the voltages V_{C1}, V_{C2}, V_{B1}, and V_{B2}.
5. Apply + ve triggering at the base of the OFF transistor and observe the Voltages V_{C1}, V_{C2}, V_{B1}, V_{B2}.

OBSERVATION:

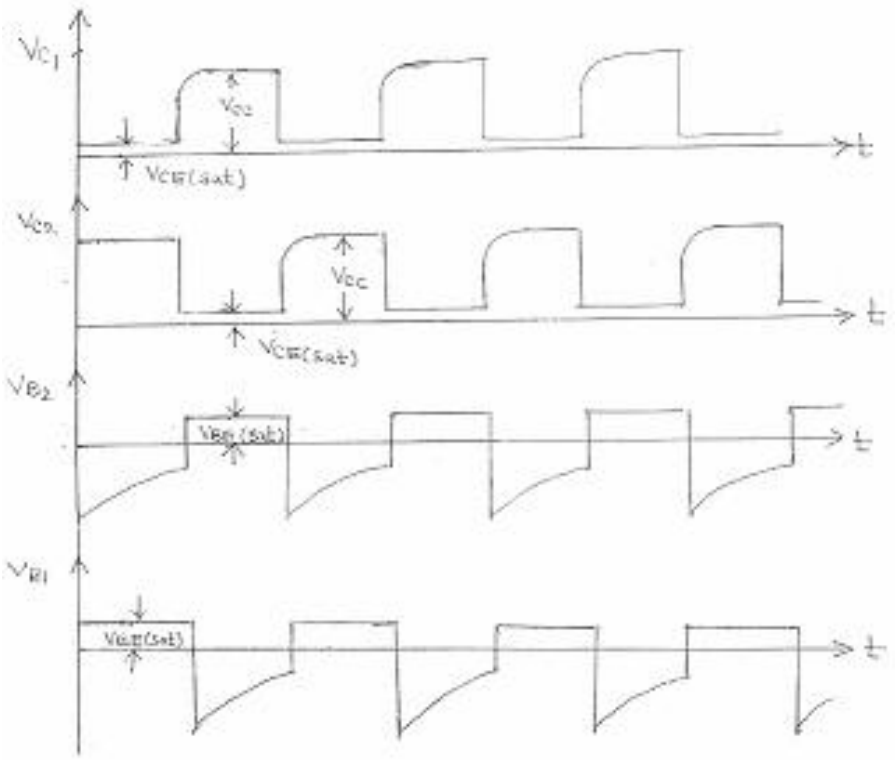
The graph of different voltages V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2} are plotted in repect of different multivibrators. The expected waveforms are shown below.



(Wavefrom of Astable Multivibrator)



(Waveform of Monostable Multivibrator)



(Waveform of Bistale Multivibrator)

PRECAUTIONS:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

CONCLUSION:

1. The different multivibrators are studied.
2. The output waveforms of different multivibrators are observed and plotted.